

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-007135

(43)Date of publication of application : 14.01.1993

(51)Int.Cl.

H03K 5/08

(21)Application number : 03-270188

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(22)Date of filing : 21.09.1991

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(30)Priority

Priority number : 02261875
02261876

Priority date : 29.09.1990
29.09.1990

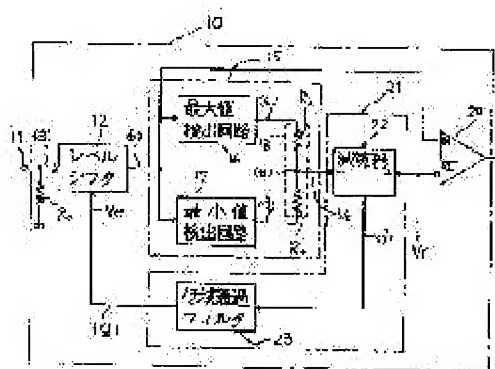
Priority country : JP
JP

(54) WAVEFORM SHAPING CIRCUIT AND DIGITAL SIGNAL ANALYZER

(57)Abstract:

PURPOSE: To apply stable waveform shaping to an inputted digital signal without being affected by its amplitude change or an offset.

CONSTITUTION: An inputted digital signal is inputted to an intermediate voltage detection circuit 15 via a level shifter 12. The intermediate voltage detection circuit 15 detects an intermediate voltage V_0 between a high level and a low level of the inputted digital signal and outputs the voltage to a subtractor 22 of a control circuit 21. The control circuit 21 outputs a difference signal between the intermediate voltage V_0 and the reference voltage V_r to the level shifter 12 via a low pass filter 25 to control the shift of the level shifter 12 in a direction that the intermediate voltage V_0 approaches the reference voltage V_r . The digital signal subjected to level shift by the level shifter 12 is inputted to a comparator 20 using the reference voltage V_r as a threshold voltage, in which the signal is subjected to waveform shaping.



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1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] A level shifter (12) which carries out variable control of the direct current offset voltage of an inputted digital signal, A comparator (20) which shapes in waveform and outputs a digital signal outputted from this level shifter as compared with predetermined reference voltage, An intermediate voltage detection means (15) to detect and output middle voltage of high-level voltage of a digital signal and low-level voltage which were outputted from said level shifter, A waveform shaping circuit provided with a control means (21) which outputs a control signal to which said direct current offset voltage is changed in response to middle voltage and said predetermined reference voltage which are outputted from this intermediate voltage detection means in order to make said middle voltage equal to said predetermined reference voltage to said level shifter.

[Claim 2] A waveform shaping circuit given [provided with holding mechanism (25) holding said control signal outputted from said control means, and the means for stopping (26) and (27) which stops an operation of said intermediate voltage detection means when said control signal is held by this holding mechanism] in the 1st paragraph.

[Claim 3] A level shifter (52) which carries out variable control of the direct current offset voltage of an inputted digital signal, A comparator (60) which shapes in waveform and outputs a digital signal outputted from this level shifter as compared with predetermined reference voltage, An intermediate voltage detector circuit (55) which detects and outputs middle voltage of high-level voltage of a digital signal and low-level voltage which were outputted from said level shifter, Middle voltage and said predetermined reference voltage which are outputted from this intermediate voltage detector circuit are received, The 1st control means (61) that outputs a control signal to which said direct current offset voltage is changed to said level shifter in order to make said middle voltage equal to said predetermined reference voltage, A variable delay device (71) which changes relatively a phase between an inputted clock signal and an output of said comparator, A discrimination circuit (72) which receives an output and said clock signal of said comparator into which a phase was relatively changed by this variable delay device, and judges numerals of an output signal of a standup of this clock signal, or said comparator at the time of falling, An error measuring instrument (75) which compares a decision signal from this discrimination circuit with a reference signal equivalent to said inputted digital signal, and outputs an error signal, A digital-signal-analysis device provided with the 2nd control means (80) that decreases said error signal which detects an almost middle delaying amount of a delaying amount from which an error signal becomes ***** with the maximum in response to an

output of this error measuring instrument, and sends out this middle delaying amount to said variable delay device, and said error measuring instrument outputs.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the digital-signal-analysis device which analyzes the waveform shaping circuit which shapes in waveform and outputs the digital signal inputted, and the digital signal inputted like a logic analyzer or an error measuring device synchronizing with a clock signal.

[0002]

[Description of the Prior Art] Generally, after shaping in waveform the digital signal inputted from the outside by the waveform shaping circuit which comprises a comparator, it comprises digital-signal-analysis devices mentioned above, such as a logic analyzer and an error measuring device, so that the binary judging may be performed.

[0003] It is necessary to set it as the best operating point which corresponds to offset of the digital signal into which the operating point of a comparator is inputted, and is not influenced by a noise in this kind of waveform shaping circuit. In order to set up this operating point, either of the following three methods was carried out conventionally.

[0004] (1) The technique of setting the threshold level (reference voltage) to a comparator as an optimum state manually, while monitoring the output wave of a comparator.

[0005] (2) A technique make the digital signal inputted input into a comparator via a capacitor, and excluding the influence of offset.

[0006] (3) A technique which carries out manual variable by a level shifter beforehand supposing the direct-current average level of the digital signal inputted, and is inputted into a comparator.

[0007] However, in (1) or (3) technique mentioned above, whenever operating point setting out by hand control is troublesome and the level of an input signal and offset change, the setting-operation must be performed.

[0008] In the technique of (2) mentioned above, the threshold which the offset voltage of the digital signal inputted into a comparator according to the mark rate (ratio of the total number of bits to generate and the number of marks contained in it) of the digital signal inputted changed and fixed cannot perform positive waveform shaping.

[0009] For this reason, the technique inputted into a comparator by making high-level voltage of the digital signal inputted and intermediate voltage of low-level voltage into a threshold is also considered.

[0010] However, in the case of the comparator of the large comparison low speed of a common mode input range, this technique is effective, but. Like the comparator for shaping the signal of ultrahigh frequency (several gigahertz) in waveform, when a common mode input range is very narrow, the comparator itself is saturated by change of the offset voltage of an input signal, and there is a problem that normal waveform-shaping operation cannot be performed.

[0011] On the other hand, the binary judging of the digital signal which shaped in waveform is performed, and the digital-signal-analysis device which analyzes the digital data is constituted as shown in drawing 17 from the former.

[0012] That is, waveform shaping of the data signal under test inputted into one input terminal 1 is carried out by the comparator 3 which makes a threshold reference voltage V_r from the

reference voltage generator 2. Since this reference voltage V_r is beforehand set as the best value by either of the techniques mentioned above, the fluctuation ingredient of the amplitude direction of the data signal under test shown in (a) of drawing 18, As shown in (b) of the figure, waveform shaping is carried out, and it is inputted into data input terminal D of the discrimination circuit 4 which comprised a D type flip-flop.

[0013]The clock signal inputted into the input terminal 5 of another side is inputted into clock terminal CP of the discrimination circuit 4 via the variable delay device 6.

[0014]This variable delay device 6 is beforehand adjusted so that a clock signal may rise to the timing whose binary level of the data signal inputted into the discrimination circuit 4 is most stable.

[0015]The output signal of the comparator 3 shown in (b) of drawing 18 as this adjustment, displaying the clock signal shown in (c) of the figure on a dual trace oscilloscope -- the standup timing of a clock signal -- the change state points I and II of a digital signal -- so that it may be located mostly at the halfway point (point that the phase margin is the largest), The method of adjusting the delaying amount of the variable delay device 6 with hand control was taken conventionally.

[0016]Thus, discernment of a binary is made to the standup timing of a clock signal of inputting the digital signal from the comparator 3 into the discrimination circuit 4, the decision output is inputted into the data analysis part 7 with a clock signal, and predetermined data analysis is conducted.

[0017]However, in such a conventional digital-signal-analysis device of composition, in addition to the hand regulation of the waveform shaping circuit mentioned above, hand regulation of the delaying amount also had to be performed, it was easy to produce the difference of these preset values according to the operator's individual difference, and there was a problem that a difference will appear also in an analysis result.

[0018]When adjusting by carrying out waveform observation with an oscilloscope, connection between apparatus is not only complicated, but by connection of an oscilloscope, the waveform of a signal may be confused and it may cause malfunction. As especially mentioned above, in connecting the cable for waveform observation to the signal of ultrahigh frequency (several gigahertz), adjustment with it becomes difficult. [this wave-like large disorder and] [exact]

[0019]For this reason, although the technique of providing the monitor terminal for waveform observation was also in the digital-signal-analysis device, there was no change in always having to prepare apparatus for waveform observation, such as an oscilloscope, and it was dramatically inconvenient.

[0020]An object of this invention is to provide the waveform shaping circuit and digital-signal-analysis device which solved the problem mentioned above.

[0021]

[Means for Solving the Problem]In order to solve said SUBJECT, a waveform shaping circuit of this invention, A level shifter (12) which carries out variable control of the direct current offset voltage of an inputted digital signal, A comparator (20) which shapes in waveform and outputs a digital signal outputted from this level shifter as compared with predetermined reference voltage, An intermediate voltage detection means (15) to detect and output middle voltage of high-level voltage of a digital signal and low-level voltage which were outputted from said level shifter, In response to middle voltage and said predetermined reference voltage which are outputted from this intermediate voltage detection means, in order to make said middle voltage equal to said predetermined reference voltage, it has a control means (21) which outputs a control signal to

which said direct current offset voltage is changed to said level shifter.

[0022]A level shifter (52) which carries out variable control of the direct current offset voltage of a digital signal into which a digital-signal-analysis device of this invention was inputted, A comparator (60) which shapes in waveform and outputs a digital signal outputted from this level shifter as compared with predetermined reference voltage, An intermediate voltage detector circuit (55) which detects and outputs middle voltage of high-level voltage of a digital signal and low-level voltage which were outputted from said level shifter, Middle voltage and said predetermined reference voltage which are outputted from this intermediate voltage detector circuit are received, The 1st control means (61) that outputs a control signal to which said direct current offset voltage is changed to said level shifter in order to make said middle voltage equal to said predetermined reference voltage, A variable delay device (71) which changes relatively a phase between an inputted clock signal and an output of said comparator, A discrimination circuit (72) which receives an output and said clock signal of said comparator into which a phase was relatively changed by this variable delay device, and judges numerals of an output signal of a standup of this clock signal, or said comparator at the time of falling, An error measuring instrument (75) which compares a decision signal from this discrimination circuit with a reference signal equivalent to said inputted digital signal, and outputs an error signal, It has the 2nd control means (80) that decreases said error signal which detects an almost middle delaying amount of a delaying amount from which an error signal becomes ***** with the maximum in response to an output of this error measuring instrument, and sends out this middle delaying amount to said variable delay device, and said error measuring instrument outputs.

[0023]

[Function]Since it is constituted in this way, in the waveform shaping circuit of this invention, the digital signal inputted is inputted into a comparator via a level shifter, and waveform shaping is carried out by predetermined reference voltage. The high-level voltage of the digital signal outputted from a level shifter and the middle voltage of low-level voltage are detected by an intermediate voltage detection means, and are outputted to a control means with reference voltage. A control means outputs a control signal for middle voltage to become equal to reference voltage to a level shifter, and changes the direct current offset voltage of the digital signal inputted.

[0024]In the digital-signal-analysis device of this invention, a phase in the meantime is changed by the variable delay device, and the clock signal inputted from the output signal and input terminal of the comparator by which waveform shaping was carried out in the waveform shaping circuit of the above-mentioned invention and the waveform shaping circuit of the identical configuration is inputted into a discrimination circuit. The decision signal from a discrimination circuit is compared with the reference signal which is equivalent to the inputted digital signal with an error measuring instrument. The error signal detected by the error measuring instrument is inputted into the 2nd control means. the delaying amount from which the delaying amount of a variable delay device is changed, and an error signal becomes ***** with the maximum while the 2nd control means receives the error signal from an error measuring instrument -- a middle delaying amount is detected mostly and it outputs to a variable delay device.

[0025]

[Example]Hereafter, the 1st example of this invention is described based on a drawing.

[0026]Drawing 1 is a circuit diagram showing the composition of the waveform shaping circuit 10 of the 1st example.

[0027]In drawing 1, the termination of the input digital signal inputted into the terminal 11 is

carried out by input-resistance R_0 (for example, 50ohms), and it is inputted into the level shifter 12.

[0028]The level shifter 12 changes the average direct-current (offset) voltage level of an input digital signal according to the size of the error signal (control signal) V_e from the control circuit 21 mentioned later. For this reason, the level shifter 12 is constituted as shown, for example in drawing 2.

[0029]That is, the average direct current voltage of an input digital signal is detected in the integration circuit by resistance R_1 and capacitor C_1 , and is inputted into the adding machine 13. The adding machine 13 adds the error signal V_e to this average direct current voltage, and outputs that added voltage via resistance R_2 . Between resistance R_2 and the terminal 11, capacitor C_2 which passes only the alternating current component of an input digital signal is provided. Therefore, from the node of capacitor C_2 and resistance R_2 , the signal with which the level was shifted only for the error voltage V_e is outputted to the signal with which the output voltage from the adding machine 13 was applied to the alternating current component of an input digital signal, i.e., an input digital signal.

[0030]Resistance R_1 and R_2 have the high resistance about [which does not have influence in the transmission impedance of 50 ohms] number 10Kohms.

[0031]The output of the level shifter 12 is inputted into the intermediate voltage detector circuit 15 and the comparator 20 mentioned later as shown in drawing 1.

[0032]The maximum detector circuit 16 where the intermediate voltage detector circuit 15 detects the maximum voltage of the output signal of the level shifter 12, It is constituted by the intermediate voltage output circuit 18 which outputs the middle voltage between the output voltage of the minimum value detecting circuit 17 which detects the minimum voltage of the output signal of the level shifter 12, and both the detector circuits 16 and 17 from the node of two resistance R_3 of the same resistance by which the series connection was carried out mutually, and R_4 .

[0033]The comparator 20 outputs high level, when the level of the output signal of the level shifter 12 inputted into one input terminal IN is larger than the predetermined reference voltage (henceforth threshold voltage) V_r applied to the input terminal REF of another side, and when small, it outputs the digital signal of a low level. This comparator 20 comprises a semiconductor device for ultrahigh frequency (for example, gallium arsenide type FET), etc.

[0034]The middle voltage V_o outputted from the intermediate voltage detector circuit 15 and the threshold voltage V_r are inputted into the control circuit 21 which is a control means of this waveform shaping circuit 10. The control circuit 21 detects the difference of the middle voltage V_o and the threshold voltage V_r which are inputted with the subtractor 22, and outputs the difference voltage signal to the level shifter 12 via the low pass filter 23, The middle voltage V_o controls the shift amount of the level shifter 12 in the direction which is in agreement with the threshold voltage V_r .

[0035]Drawing 3 shows an example of the more concrete circuit of the intermediate voltage detector circuit 15 and the control circuit 21.

[0036]Namely, the diode 16a by which the anode side was connected to the output of the level shifter 12 in the maximum detector circuit 16, It has the Masakata-oriented peak detection circuit formed by the capacitor 16b connected with the cathode of the diode 16a between groundings, Between the node of this diode 16a and capacitor 16b, and predetermined negative supply- V_1 , the constant current source 16c which sends very small forward bias current is connected to the diode 16a.

[0037]The diode 17a by which the cathode side was connected to the output of the level shifter 12 in the minimum value detecting circuit 17, It has a peak detection circuit of the negative direction formed by the capacitor 17b connected between the anode side of the diode 17a, and grounding, Between the node of the diode 17a and the capacitor 17b, and predetermined positive supply $+V_1$, the constant current source 17c which sends very small forward bias current is connected to the diode 17a.

[0038]Therefore, from the node of the diode 16a of the maximum detector circuit 16, and the capacitor 16b, The high-level voltage more than negative supply- V_1 voltage will be outputted among the digital signals outputted from the level shifter 12, and the low-level voltage below positive supply $+V_1$ voltage will be outputted from the node of the diode 17a of the minimum value detecting circuit 17, and the capacitor 17b.

[0039]The forward bias current from the constant current sources 16c and 17c over each diodes 16a and 17a hardly affects it to an input digital signal, but is set as the current value about [required to compensate the nonlinearity of detection operation of each diodes 16a and 17a moreover] 1microA.

[0040]The capacity value of the capacitors 16c and 17c is set as the value of about 1000 PF which can hold the peak value of the digital signal of 1 kHz or more of cycle periods in consideration of the forward bias current over each diodes 16a and 17a being a 1microA grade.

[0041]The subtractor 22 of the control circuit 21 is formed of the differential amplifier 22a and the feedback resistor 22b, and the voltage according to the difference of the intermediate voltage V_o and the threshold voltage V_r is outputted from the differential amplifier 22a. The low pass filter 23 formed by the resistance 23a and the capacitor 23b outputs the error signal V_e excluding the noise component from the output of the differential amplifier 22a to the level shifter 12.

[0042]Therefore, since the output voltage of the differential amplifier 22a will rise if the middle voltage V_o falls to the threshold voltage V_r , the level of the digital signal which the error signal V_e goes up and is outputted from the level shifter 12 goes up to the whole. Conversely, since the output voltage of the differential amplifier 22a will decline if the middle voltage V_o rises to the threshold voltage V_r , the level of the digital signal which the error signal V_e falls and is outputted from a level shifter will fall to the whole.

[0043]Next, operation of the above-mentioned waveform shaping circuit 10 is explained.

[0044]Now, temporarily, the maximum of the digital signal inputted to the level shifter 12 by time t_0 and the mean value of the minimum presuppose that it is equal to the threshold voltage V_r of the comparator 20, as shown in (a) of drawing 4.

[0045]In this case, since the output of the subtractor 22 of the control circuit 21 serves as zero, the digital signal inputted into the level shifter 12 is inputted into the comparator 20 as it is, and waveform shaping is carried out on the threshold voltage V_r .

[0046]And in time t_1 , as shown in (a) of drawing 4, the direct current offset voltage of the digital signal inputted presupposes that it went up to step form. As the output signal of the level shifter 12 is also shown in (b) of the figure according to this, an ascending change is carried out, and as the output voltage of the minimum value detecting circuit 17 in the maximum detector circuit 16 of the intermediate voltage detector circuit 15 is also shown in (c) of the figure, and (d), it changes to step form.

[0047]For this reason, as the middle voltage V_o to the subtractor 22 is also shown in (e) of the figure, it changes to step form, and the output of the subtractor 22 changes in the minus direction a lot, as shown in (f) of the figure.

[0048]Therefore, from the low pass filter 23, as shown in (g) of the figure, the error signal V_e

which descends at the speed according to the damping time constant is outputted.

[0049]For this reason, since the shift amount of the level shifter 12 also increases to the minus side at ****, the mean value of the digital signal inputted into the comparator 20 changes in the direction which is in agreement with the threshold voltage V_r , as shown in (b) of the figure.

[0050]As a result, in time t_2 , the difference between the input voltage of the subtractor 22 is set to about 0, this stable state is continued henceforth, and the digital signal by which waveform shaping was carried out certainly is acquired from the output of the comparator 20.

[0051]Henceforth, even if offset of an input digital signal changes, since feedback control is always carried out in the direction approaching the threshold voltage V_r , positive waveform-shaping operation stabilizes for it and continues the middle voltage of the digital signal inputted into a comparator.

[0052]

[The 2nd example] Although the control loop for controlling the shift amount of the level shifter 12 was always closed in said 1st example, After stabilizing the shift amount to an input digital signal and becoming an appropriate amount, while holding this shift amount and opening a loop, it can also constitute so that detection operation of the intermediate voltage detector circuit 15 connected to the signal line may be stopped.

[0053]Drawing 5 shows the composition of this hold type waveform shaping circuit 10' which is the 2nd example. The hold circuit 25 where this waveform shaping circuit 10' holds the size of an error signal in response to a hold signal (stop signal), It has the switches 26 and 27 (means for stopping) which close with a hold signal (stop signal) and give reverse-bias-voltage** V_2 to the diodes 16a and 17a of the minimum value detecting circuit 17 in the maximum detector circuit 16.

[0054]In waveform shaping circuit 10' constituted in this way. If the shift amount of the level shifter 12 to an input digital signal inputs a hold signal (stop signal) after turning into an appropriate amount by said same loop control, The value of the error signal V_e which gives a proper shift amount is held by the hold circuit 25, and the shift amount of the level shifter 12 is fixed to an appropriate amount. Since the diodes 16a and 17a of both the detector circuits 16 and 17 of the intermediate voltage detector circuit 15 are electrically separated by reverse bias voltage from the line of a digital signal at this time, the adverse effect (aggravation of a high frequency characteristic) of diode connection to this line can be prevented.

[0055]Although the hold signal explained the case where reverse bias voltage** V_2 was only impressed to the maximum detector circuit 16 and the minimum value detecting circuit 17, in waveform shaping circuit 10' shown in drawing 5, Like the intermediate voltage detector circuit 15 which showed drawing 3 the example, when the very small current of the forward direction is being added from the constant current sources 16c and 17c to the diodes 16a and 17a, a hold signal may be made to perform a change with this constant current source and reverse-bias-voltage** V_2 .

[0056]Drawing 6 shows the concrete circuitry of the stop circuit 29 which stops detection operation of the intermediate voltage detector circuit 15 by switching the constant current sources 16c and 17c and reverse-bias-voltage** V_2 .

[0057]This stop circuit 29 switches switch 26' and 27' to a hold / limiting circuit mode from a normal mode, in response to the fact that [the above-mentioned hold signal] as a stop signal. In a normal mode, since [said] very small forward bias current is similarly supplied from the constant current sources 16c and 17c, the intermediate voltage detector circuit 15 performs detection of the maximum of the digital signal from the level shifter 12, and the minimum to the

diodes 16a and 17a.

[0058]In a hold mode, since reverse-bias-voltage V_2 larger (for example, about 4 volts) enough than the maximum of an input digital signal and the minimum is added to the diodes 16a and 17a, the intermediate voltage detector circuit 15 suspends the detecting operation of the maximum and the minimum.

[0059]in limiting circuit mode -- the forward voltage drop of the diodes 16a and 17a -- receiving an input digital signal, since about 1.3 volts reverse-bias-voltage V_2 which expected 0.7 volt per part is added to the diodes 16a and 17a -- about -- a limiting circuit can be applied by $2V$.

[0060]As mentioned above, by carrying out variable control of the voltage set up as reverse-bias-voltage V_2 in the circuit of drawing 6, so that it may become 4 volts or 1.3 volts according to the state at that time, It can be used with an above-mentioned normal mode, being able to switch both a hold mode or limiting circuit mode. In drawing 6, the numerals 16d and 17d are buffer amplifier, respectively.

[0061]If the stop circuit 29 is constituted as shown in drawing 7, it will become possible to carry out limiter operation of the diodes 16a and 17a in any [of the above-mentioned normal mode and a hold mode] case.

[0062]In the stop circuit 29 shown in drawing 7, about 0.6 volt reverse-bias-voltage V_3 is always impressed via the diodes 30 and 31 to the diodes 16a and 17a. The constant current source 17c by the side of the minimum value detecting circuit 17 is connected to the hold side of switch 26' by the side of the maximum detector circuit 16, and the constant current source 16c by the side of the maximum detector circuit 16 is connected to the hold side of switch 27' by the side of the minimum value detecting circuit 17.

[0063]For this reason, at the time of a normal mode, it is the same as that of the case of the circuit of said drawing 6 that the forward bias from each constant current source 16c and 17c is applied to the diodes 16a and 17a, and the maximum to an input digital signal and minimum detection are performed.

[0064]However, in this normal mode, if the output voltage from the level shifter 12 becomes lower than $-2V$, since the diode 17a and the diode 31 of the minimum value detecting circuit 17 flow, the minimum value detecting circuit 17 side will require a limiting circuit in $-2V (-V_3 - 1.4V)$.

[0065]In a normal mode, since the diode 16a and the diode 30 by the side of the maximum detector circuit 16 will flow if the output voltage from the level shifter 12 becomes higher than $+2V$, the maximum detector circuit 16 side will require a limiting circuit in $+2V (+V_3 + 1.4V)$.

[0066]Above $-1.4V$ is a part for the voltage drop in the diodes 17a and 31, and $+1.4V$ is a part for the voltage drop in the diodes 16a and 30.

[0067]In the time of a hold mode, as for the diodes 16a and 17a, the maximum to an input digital signal and minimum detecting operation are suspended by the constant current source 17c and the reverse bias from the [16] side, respectively.

[0068]However, in this hold mode, if it is set as about $V_1 = 1.3V$, If the output voltage from the level shifter 12 becomes lower than $-2V$ or it becomes higher than $+2V$, a limiting circuit will come to start in $-2V$ or $+2V$ like the time of the normal mode mentioned above, respectively.

[0069]As the above mentioned hold circuit 25 of drawing 5, drawing 6, and drawing 7, as shown in drawing 8, a digital type hold circuit other than an analog type hold circuit can also be used.

[0070]The hold circuit 25 shown in drawing 8 changes the error signal V_e from the control circuit 21 into digital value with A/D converter 32, and memorizes digital value when a hold signal (switching signal) is inputted to the memory circuit 33. The digital value memorized by

the memory circuit 33 is changed into analog voltage by D/A converter 34, and is outputted to the level shifter 12 via the switch 35 by it.

[0071]The switching circuit 35 outputs the error signal from the control circuit 21 to the level shifter 12 as it is, when the hold signal is not inputted, and when the hold signal is inputted, it outputs the signal from D/A converter 34. In order that there may be no change of a hold output compared with an analog type hold circuit, such a digital type hold circuit is advantageous when prolonged hold operation is required.

[0072]Although the subtractor 22 and the low pass filter 23 were made another composition as a concrete circuit of the control circuit 21 in said explanation, as shown in drawing 9, a control circuit can also be simplified using the found the integral type circuit which returns the output of the operational amplifier 21a by the capacitor 21b.

[0073]In said example to know the shift amount in the level shifter 12. If the size of the error signal V_e is read with a voltmeter, or the difference of the average direct current voltage during input and output of the level shifter 12 detected in the integration circuit of resistance R_5 and capacitor C_5 , respectively is read with the voltmeter 37 as shown in drawing 10, the shift amount of the level shifter 12 can be known. The threshold level of an input digital signal can be known from this level shift quantity. Since the shift amount in the level shifter 12 can be detected with A/D converter 32 when the digital type hold circuit 25 shown in drawing 8 is used, a circuit like drawing 10 is unnecessary.

[0074]Although said example explained the waveform shaping circuit used by ultrahigh frequency, it can apply the waveform shaping circuit of this invention also to the waveform shaping circuit of a low frequency band.

[0075]As a comparator, what [not only] comprised gallium arsenide type FET of said example but the comparator which comprised a silicon bipolar transistor and a hetero-bipolar transistor (HBT), for example may be used. Various things, such as a level shifter which comprised a blocking capacitor and high frequency blocking coil other than the composition of said example also about the level shifter, can be used.

[0076]

[The 3rd example] Next, the digital-signal-analysis device using the above waveform shaping circuits is explained.

[0077]Drawing 11 is a block diagram showing the composition at the time of mistaking the digital-signal-analysis device of this invention, and applying to a measuring device as the 3rd example.

[0078]After this error measuring device shapes in waveform the data signal under test inputted with a clock signal, It is constituted so that it may compare with the data of the reference signal equivalent to the digital signal into which it identified to the timing in sync with the clock signal into which the binary judging was inputted, and the identified signal was inputted.

[0079]A data signal under test is inputted into the waveform shaping circuit 10 of drawing 1 and the waveform shaping circuit 50 of an identical configuration which were mentioned above.

[0080]That is, the termination of the data signal under test inputted from the input terminal 51 is carried out by input-resistance R_0 (for example, 50ohms), and it is inputted into the level shifter 52. The level shifter 52 changes the direct-current average (offset) voltage of the inputted data signal under test according to the size of the error signal V_e .

[0081]The output of the level shifter 52 is inputted into the intermediate voltage detector circuit 55 and the comparator 60. The intermediate voltage detector circuit 55 the high-level peak voltage of a digital signal and the peak voltage of a low level which are outputted from the level

shifter 52, It detects in the high-level peak detection circuit (maximum detector circuit) 56 and the low-level peak detection circuit (minimum value detecting circuit) 57, respectively, and the middle voltage V_o is outputted from the middle point of two equal resistance R .

[0082]This middle voltage V_o is inputted into the 1st control circuit 61 with the reference voltage (threshold voltage) V_r from the reference voltage generator 59.

[0083]The 1st control circuit 61 that is the 1st control means, The low pass filter which outputs the error signal V_e which integrated with and obtained the subtraction output of the subtractor circuit 62 which detects the difference of the reference voltage V_r and the middle voltage V_o , and the subtractor circuit 62. (It is hereafter described as LPF) It comprises 63 and the middle voltage V_o carries out feedback control of the shift amount of the level shifter 52 in the direction which always approaches the reference voltage V_r .

[0084]High level and when low [the digital signal outputted from the level shifter 52 is higher than the reference voltage V_r and], it outputs the digital signal of a low level, and the comparator 60 shapes the inputted digital signal in waveform.

[0085]As mentioned above, the above composition shall completely be the same as that of the waveform shaping circuit 10 shown in drawing 1, and shall be based on the above-mentioned explanation about the details and the modification of each part.

[0086]On the other hand, the clock signal inputted into the input terminal 70 is inputted into the error test section 75 which are the discrimination circuit 72 and an error measuring instrument via the variable delay device 71. The variable delay device 71 is delayed according to a control signal in the clock signal inputted, and changes relatively the phase of the clock signal over a data signal under test. As this variable delay device 71, the thing of variable-length slab line structure which changes that delaying amount is used as an object for ultrahigh frequency by carrying out slag variable [of the signal line length].

[0087]The discrimination circuit 72 carries out a binary judging in the timing of the standup (or falling) of the clock signal into which the level of the digital signal outputted from the comparator 60 is inputted from the variable delay device 71, and outputs the discernment output to the error test section 75.

[0088]The error test section 75 which is a data analysis part of the error measuring device by this example is constituted by the criterion data generator 76, the code comparison machine 77, the inharmonic counter 78, and the clock counter 79.

[0089]The criterion data generator 76 outputs the criterion data of the same pattern as the data which it is going to measure to the code comparison machine 77 to the timing in sync with the clock signal from the variable delay device 71.

[0090]The code comparison machine 77 of numerals of the output of the discrimination circuit 72 and criterion data corresponds, judges disagreement, and when inharmonic, it outputs a dissidence signal to the inharmonic counter 78.

[0091]While having received the gating signal from the control section 80 mentioned later, the inharmonic counter 78 continues calculation of a dissidence signal, and is performed. The clock counter 79 calculates the clock signal outputted from the variable delay device 71, while having received the gating signal from the control section 80.

[0092]The control section 80 which is the 2nd control means of this error measuring device comprises a microprocessor (CPU) etc., and mainly has two mode management.

[0093]That is, the 1st mode management is the usual measuring process which reads the counting result of both counters, calculates a digital error rate, and displays the result on the display for indication 81, after carrying out predetermined time calculation of the inharmonic

counter 78 and the clock counter 79 simultaneously. The 2nd mode management is the optimal delaying amount detection processing which detects the delaying amount from which carries out prescribed range per-continuum variable [of the delaying amount to the clock signal of the variable delay device 71], and asks for the error rate data to the delaying amount, it memorizes in the memory 80a, and an error rate serves as the minimum before a measuring process.

[0094]A/D converter 65 in drawing 11 changes the error signal V_e from the 1st control circuit 61 of the waveform shaping circuit 50 into digital value, and outputs this value to the control section 80 as a shift amount of the level shifter 52. The control section 80 memorizes this shift amount in the memory 80a, or displays it on the display for indication 81.

[0095]Next, operation of this error measuring device is explained.

[0096]If a data signal under test and a clock signal are inputted into the input terminals 51 and 70, respectively, the waveform shaping circuit 50 will control a shift amount in the direction which coincides the middle voltage V_o of the high level of the inputted data signal under test, and a low level with the reference voltage V_r .

[0097]This operation is completely the same as the operation explained by above-mentioned drawing 4.

[0098]For this reason, from the comparator 60, as shown in (a) of drawing 12, waveform shaping is carried out on the threshold voltage (reference voltage) V_r , and the data signal under test which does not have fluctuation in an amplitude direction is outputted.

[0099]It can be checked by displaying the shift amount from A/D converter 65 on the display for indication 81, or performing the stable decision processing for oneself [control-section 80] that the shift amount of the level shifter 52 has been stabilized.

[0100]Next, the control section 80 performs the optimal delaying amount detection processing mentioned above.

[0101]That is, the control section 80 asks for the cycle T of a clock signal from the counting result, after inputting a gating signal into the predetermined time clock counter 79. And changing the delaying amount of the variable delay device 71 from initial value D_0 to one cycle of a clock signal at least at the predetermined step d , as shown in (b₁) of drawing 12, (b₂), and (b₃), an error rate is searched for for every predetermined step, and the result is memorized in the memory 80a.

[0102](c) of drawing 12 shows change of the error rate over change of the delaying amount memorized by the memory 80a. As opposed to the output signal ((a) of the figure) of the comparator 60 which has fluctuation in a phase constituent so that clearly from this figure, Change of an error rate when the standup timing of a clock signal is changed by 1.5 cycles from (b₁) of the figure to (b₃) of the figure serves as the maximum at the change state point of the output signal of the comparator 60, and two places of the maximum points are obtained.

[0103]The control section 80 sets automatically mean value D_{40} of delaying amount D_2 [from which an error rate serves as the maximum], and D_6 as the variable delay device 71 as optimal delaying amount that has the phase margin most based on the data of the memorized error rate.

[0104]After performing the above setting out, the control section 80 performs the usual error measuring process, and displays the measured error rate on the display for indication 81 one by one.

[0105]The threshold level of the data signal under test computed from the reference voltage V_r to level shift quantity, and this level shift quantity and comparator 60 from A/D converter 65 is also displayed on the display for indication 81 at any time.

[0106]Although the subtraction result of middle voltage and reference voltage was inputted into the level shifter 52 via LPF63 in the error measuring device of this 3rd example, As shown in

drawing 13, digital conversion of the subtraction result is carried out to subtraction data with A/D converter 65, A shift amount for this subtraction data to approach zero may be computed by the operation control part 90, and this computed shift amount data may be sent out to D/A converter 66, and it may constitute so that the shift amount of the level shifter 52 may be controlled. This operation control part 90 is constituted by one CPU with the control section 80. [0107]The A/D conversion of the middle voltage outputted from the intermediate voltage detector circuit 55 is carried out directly, It is also possible to constitute so that it may send to the operation control part 90 and shift amount data corresponding this intermediate voltage data to that difference as compared with reference voltage data may be outputted to the level shifter 52 via D/A converter 65 by the operation control part 90. In this case, the operation control part 90 serves as the 1st control means.

[0108]In said 3rd example, in order to set up the optimal delaying amount to a clock signal, had determined the optimum value from the maximum of the error rate acquired by changing a delaying amount over the above by one cycle of a clock signal, but. It may be made for an error rate to set up the delaying amount used as the minimum as an optimum value as it is. This is an effective method, when fluctuation of the phase of an input appearance signal is large and the flat part between $D_{of(c)5}$ from D_3 of drawing 12 is very narrow.

[0109]It may be made to set up the mean value of two delaying amounts (for example, D_3 of drawing 12, D_5) which give the greatest not an error rate but equal error rate like said example as optimal delaying amount.

[0110]By operating the input means of the switch etc. which were formed in the display for indication, After starting a series of operations which set up the optimal threshold voltage of a data signal under test and completing the operation, operation which sets up the optimal delaying amount is performed and it may be made to display the threshold level and the delaying amount which were set up on a display for indication.

[0111]In said 3rd example, although the phase by the side of a clock signal was delayed, this may not limit this invention, and as shown, for example in drawing 14, it may form the variable delay device 71 between the input terminal 51 by the side of a data signal under test, and the level shifter 52. The variable delay device 71 may be formed between the level shifter 52 and the comparator 60 or between the comparator 60 and the discrimination circuit 72.

[0112]Although the waveform shaping circuit 10 shown in drawing 1 and the waveform shaping circuit 50 of the identical configuration were performing waveform shaping of the input signal in said 3rd example, Waveform shaping circuit 10' of the 2nd example (drawing 5) which has a hold facility of a shift amount and an operation stop function of the intermediate voltage detector circuit 55 may be used. The circuit which has the limiter function similarly shown in above-mentioned drawing 6 as a modification of drawing 5 and drawing 7 may be used.

[0113]The circuit of drawing 13 mentioned above may be transformed still like drawing 15, and the digital type hold circuit explained by above-mentioned drawing 8 may be formed.

[0114]It judges itself that the loop of the waveform shaping circuit 50 was stabilized as for the operation control part 90 of this composition, and it became the optimal shift amount, While outputting a hold signal (stop signal) to the switching circuit 35 and the stop circuit 69 and carrying out fixed setting out of the optimal shift amount to the level shifter 52, the detecting operation of the intermediate voltage detector circuit 55 is stopped (in addition, the stop circuit 69 consists of the same composition as the above-mentioned stop circuit 29).

[0115]The operation control part 90 which performs setting-out control of the optimal shift amount to the level shifter 52, and stop control of intermediate voltage detecting operation in this

way, If the control section 80 which performs setting-out control of the optimal delaying amount to the variable delay device 71 is constituted from one CPU, A series of programs can be made to perform the setting processing of the optimal shift amount and the setting processing of the optimal delaying amount continuously, [as opposed to a data signal under test by easy key operation etc.] And there is an advantage that transfer of data with other devices can be easily performed using the communication function of CPU.

[0116]Drawing 16 is an example of the device which shows the more concrete example of the error measuring device of the 3rd example of this invention, and performs error measurement of the data signal of ultrahigh frequency under test especially.

[0117]In drawing 16, the input clock applied to the input data applied to the waveform shaping circuit 101 and the variable delay device 102 is rationalized as mentioned above, respectively, and it is outputted to the discrimination circuit 103.

[0118]The data in which discernment which was mentioned above by this discrimination circuit 103 was made is demultiplexed by $1/N$ in the $1/N$ demultiplexer 104 with the $1/N$ clock by which it is generated from the timing generation part 105 based on the output clock of the variable delay device 102. For example, in the case of $N=32$, input data is demultiplexed by 310 MHz at 10 GHz, and error detection of the input data is carried out by the error detection part 106 as 32-channel data. this error result -- an error -- calculation -- it is sent to the indicator 108 and the synchronous controlling part 109 via the part 107. The reference pattern generating part 110 generates the standard pattern information for giving the error detection part 106 according to the output from this synchronous controlling part 109.

[0119]this error detection part 106, the reference pattern generating part 110, and an error -- calculation -- the part 107 and the synchronous controlling part 109 are controlled by the $1/N$ clock from the timing generation part 105. The control section 111 which comprises a CPU controls each part. The auto search part 112 controls the waveform shaping circuit 101 and the variable delay device 102 in the respectively proper state as well as said each example under control of the control section 111.

[0120]In this error measuring device, since the data signal identified to the optimal timing is divided into the parallel data of the speed of $1/N$ and an error judging is carried out by the discrimination circuit 103 like said example, error measurement of the data signal of ultrahigh frequency can be ensured.

[0121]The above-mentioned example is applicable like other digital analysis devices, such as a logic analyzer, although the example which mistook the digital-signal-analysis device of this invention, and was applied to the measuring device was explained.

[0122]

[Effect of the Invention]As explained above, the waveform shaping circuit of this invention, The direct current offset voltage of an input digital signal, i.e., the middle voltage of the high-level voltage of the output signal of a level shifter, and low-level voltage. The shift amount of a level shifter is controlled in the direction put close to a predetermined threshold, and it is constituted so that the output signal of the level shifter may be shaped in waveform with a predetermined threshold.

[0123]For this reason, without carrying out troublesome waveform observation and hand regulation, the center of the amplitude of the digital signal inputted into a comparator is driven into the state where it was always in agreement with the predetermined threshold, and positive waveform shaping can be performed.

[0124]A shift amount can be fixed to an appropriate amount and it is effective in not worsening

the high frequency characteristic of a signalling channel in the holding circuit holding the size of the error signal over a level shifter, and the waveform shaping circuit in which the means for stopping which stops operation of an intermediate voltage detector circuit was provided.

[0125]Based on the error measurement result obtained by the digital-signal-analysis device of this invention carrying out prescribed range delay variable [of the phase of the digital signal and clock signal which are outputted from said waveform shaping circuit] relatively like said explanation, A delaying amount for the timing of discernment to go into the optimal position between the change state points that the digital signal inputted into a discrimination circuit adjoins each other is detected from a comparator, and it is constituted so that the delaying amount may be set as a variable delay device.

[0126]For this reason, the operating point and identification timing of waveform shaping by a comparator can be set as an optimum state in the state where there are no wave-like error and individual difference by disorder, without carrying out the voltage adjustment and phase adjustment operation by complicated hand control while carrying out waveform observation.

TECHNICAL FIELD

[Industrial Application]This invention relates to the digital-signal-analysis device which analyzes the waveform shaping circuit which shapes in waveform and outputs the digital signal inputted, and the digital signal inputted like a logic analyzer or an error measuring device synchronizing with a clock signal.

EFFECT OF THE INVENTION

[Effect of the Invention]As explained above, the waveform shaping circuit of this invention, The direct current offset voltage of an input digital signal, i.e., the middle voltage of the high-level voltage of the output signal of a level shifter, and low-level voltage. The shift amount of a level shifter is controlled in the direction put close to a predetermined threshold, and it is constituted so that the output signal of the level shifter may be shaped in waveform with a predetermined threshold.

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comparator can be set as an optimum state in the state where there are no wave-like error and individual difference by disorder, without carrying out the voltage adjustment and phase adjustment operation by complicated hand control while carrying out waveform observation.

TECHNICAL PROBLEM

[Description of the Prior Art] Generally, after shaping in waveform the digital signal inputted from the outside by the waveform shaping circuit which comprises a comparator, it comprises digital-signal-analysis devices mentioned above, such as a logic analyzer and an error measuring device, so that the binary judging may be performed.

[0003] It is necessary to set it as the best operating point which corresponds to offset of the digital signal into which the operating point of a comparator is inputted, and is not influenced by a noise in this kind of waveform shaping circuit. In order to set up this operating point, either of the following three methods was carried out conventionally.

[0004] (1) The technique of setting the threshold level (reference voltage) to a comparator as an optimum state manually, while monitoring the output wave of a comparator.

[0005] (2) A technique make the digital signal inputted input into a comparator via a capacitor, and excluding the influence of offset.

[0006] (3) A technique which carries out manual variable by a level shifter beforehand supposing the direct-current average level of the digital signal inputted, and is inputted into a comparator.

[0007] However, in (1) or (3) technique mentioned above, whenever operating point setting out by hand control is troublesome and the level of an input signal and offset change, the setting-operation must be performed.

[0008] In the technique of (2) mentioned above, the threshold which the offset voltage of the digital signal inputted into a comparator according to the mark rate (ratio of the total number of bits to generate and the number of marks contained in it) of the digital signal inputted changed and fixed cannot perform positive waveform shaping.

[0009] For this reason, the technique inputted into a comparator by making high-level voltage of the digital signal inputted and intermediate voltage of low-level voltage into a threshold is also considered.

[0010] However, in the case of the comparator of the large comparison low speed of a common mode input range, this technique is effective, but. Like the comparator for shaping the signal of ultrahigh frequency (several gigahertz) in waveform, when a common mode input range is very narrow, the comparator itself is saturated by change of the offset voltage of an input signal, and there is a problem that normal waveform-shaping operation cannot be performed.

[0011] On the other hand, the binary judging of the digital signal which shaped in waveform is performed, and the digital-signal-analysis device which analyzes the digital data is constituted as shown in drawing 17 from the former.

[0012] That is, waveform shaping of the data signal under test inputted into one input terminal 1 is carried out by the comparator 3 which makes a threshold reference voltage V_r from the reference voltage generator 2. Since this reference voltage V_r is beforehand set as the best value by either of the techniques mentioned above, the fluctuation ingredient of the amplitude direction of the data signal under test shown in (a) of drawing 18, As shown in (b) of the figure, waveform shaping is carried out, and it is inputted into data input terminal D of the discrimination circuit 4 which comprised a D type flip-flop.

[0013] The clock signal inputted into the input terminal 5 of another side is inputted into clock

terminal CP of the discrimination circuit 4 via the variable delay device 6.

[0014]This variable delay device 6 is beforehand adjusted so that a clock signal may rise to the timing whose binary level of the data signal inputted into the discrimination circuit 4 is most stable.

[0015]The output signal of the comparator 3 shown in (b) of drawing 18 as this adjustment, displaying the clock signal shown in (c) of the figure on a dual trace oscilloscope -- the standup timing of a clock signal -- the change state points I and II of a digital signal -- so that it may be located mostly at the halfway point (point that the phase margin is the largest), The method of adjusting the delaying amount of the variable delay device 6 with hand control was taken conventionally.

[0016]Thus, discernment of a binary is made to the standup timing of a clock signal of inputting the digital signal from the comparator 3 into the discrimination circuit 4, the decision output is inputted into the data analysis part 7 with a clock signal, and predetermined data analysis is conducted.

[0017]However, in such a conventional digital-signal-analysis device of composition, in addition to the hand regulation of the waveform shaping circuit mentioned above, hand regulation of the delaying amount also had to be performed, it was easy to produce the difference of these preset values according to the operator's individual difference, and there was a problem that a difference will appear also in an analysis result.

[0018]When adjusting by carrying out waveform observation with an oscilloscope, connection between apparatus is not only complicated, but by connection of an oscilloscope, the waveform of a signal may be confused and it may cause malfunction. As especially mentioned above, in connecting the cable for waveform observation to the signal of ultrahigh frequency (several gigahertz), adjustment with it becomes difficult. [this wave-like large disorder and] [exact]

[0019]For this reason, although the technique of providing the monitor terminal for waveform observation was also in the digital-signal-analysis device, there was no change in always having to prepare apparatus for waveform observation, such as an oscilloscope, and it was dramatically inconvenient.

[0020]An object of this invention is to provide the waveform shaping circuit and digital-signal-analysis device which solved the problem mentioned above.

MEANS

[Means for Solving the Problem]In order to solve said SUBJECT, a waveform shaping circuit of this invention, A level shifter (12) which carries out variable control of the direct current offset voltage of an inputted digital signal, A comparator (20) which shapes in waveform and outputs a digital signal outputted from this level shifter as compared with predetermined reference voltage, An intermediate voltage detection means (15) to detect and output middle voltage of high-level voltage of a digital signal and low-level voltage which were outputted from said level shifter, In response to middle voltage and said predetermined reference voltage which are outputted from this intermediate voltage detection means, in order to make said middle voltage equal to said predetermined reference voltage, it has a control means (21) which outputs a control signal to which said direct current offset voltage is changed to said level shifter.

[0022]A level shifter (52) which carries out variable control of the direct current offset voltage of a digital signal into which a digital-signal-analysis device of this invention was inputted, A comparator (60) which shapes in waveform and outputs a digital signal outputted from this level

shifter as compared with predetermined reference voltage, An intermediate voltage detector circuit (55) which detects and outputs middle voltage of high-level voltage of a digital signal and low-level voltage which were outputted from said level shifter, Middle voltage and said predetermined reference voltage which are outputted from this intermediate voltage detector circuit are received, The 1st control means (61) that outputs a control signal to which said direct current offset voltage is changed to said level shifter in order to make said middle voltage equal to said predetermined reference voltage, A variable delay device (71) which changes relatively a phase between an inputted clock signal and an output of said comparator, A discrimination circuit (72) which receives an output and said clock signal of said comparator into which a phase was relatively changed by this variable delay device, and judges numerals of an output signal of a standup of this clock signal, or said comparator at the time of falling, An error measuring instrument (75) which compares a decision signal from this discrimination circuit with a reference signal equivalent to said inputted digital signal, and outputs an error signal, It has the 2nd control means (80) that decreases said error signal which detects an almost middle delaying amount of a delaying amount from which an error signal becomes ***** with the maximum in response to an output of this error measuring instrument, and sends out this middle delaying amount to said variable delay device, and said error measuring instrument outputs.

OPERATION

[Function] Since it is constituted in this way, in the waveform shaping circuit of this invention, the digital signal inputted is inputted into a comparator via a level shifter, and waveform shaping is carried out by predetermined reference voltage. The high-level voltage of the digital signal outputted from a level shifter and the middle voltage of low-level voltage are detected by an intermediate voltage detection means, and are outputted to a control means with reference voltage. A control means outputs a control signal for middle voltage to become equal to reference voltage to a level shifter, and changes the direct current offset voltage of the digital signal inputted.

[0024] In the digital-signal-analysis device of this invention, a phase in the meantime is changed by the variable delay device, and the clock signal inputted from the output signal and input terminal of the comparator by which waveform shaping was carried out in the waveform shaping circuit of the above-mentioned invention and the waveform shaping circuit of the identical configuration is inputted into a discrimination circuit. The decision signal from a discrimination circuit is compared with the reference signal which is equivalent to the inputted digital signal with an error measuring instrument. The error signal detected by the error measuring instrument is inputted into the 2nd control means. the delaying amount from which the delaying amount of a variable delay device is changed, and an error signal becomes ***** with the maximum while the 2nd control means receives the error signal from an error measuring instrument -- a middle delaying amount is detected mostly and it outputs to a variable delay device.

EXAMPLE

[Example] Hereafter, the 1st example of this invention is described based on a drawing.

[0026] Drawing 1 is a circuit diagram showing the composition of the waveform shaping circuit 10 of the 1st example.

[0027] In drawing 1, the termination of the input digital signal inputted into the terminal 11 is

carried out by input-resistance R_0 (for example, 50ohms), and it is inputted into the level shifter 12.

[0028]The level shifter 12 changes the average direct-current (offset) voltage level of an input digital signal according to the size of the error signal (control signal) V_e from the control circuit 21 mentioned later. For this reason, the level shifter 12 is constituted as shown, for example in drawing 2.

[0029]That is, the average direct current voltage of an input digital signal is detected in the integration circuit by resistance R_1 and capacitor C_1 , and is inputted into the adding machine 13. The adding machine 13 adds the error signal V_e to this average direct current voltage, and outputs that added voltage via resistance R_2 . Between resistance R_2 and the terminal 11, capacitor C_2 which passes only the alternating current component of an input digital signal is provided. Therefore, from the node of capacitor C_2 and resistance R_2 , the signal with which the level was shifted only for the error voltage V_e is outputted to the signal with which the output voltage from the adding machine 13 was applied to the alternating current component of an input digital signal, i.e., an input digital signal.

[0030]Resistance R_1 and R_2 have the high resistance about [which does not have influence in the transmission impedance of 50 ohms] number 10Komega.

[0031]The output of the level shifter 12 is inputted into the intermediate voltage detector circuit 15 and the comparator 20 mentioned later as shown in drawing 1.

[0032]The maximum detector circuit 16 where the intermediate voltage detector circuit 15 detects the maximum voltage of the output signal of the level shifter 12, It is constituted by the intermediate voltage output circuit 18 which outputs the middle voltage between the output voltage of the minimum value detecting circuit 17 which detects the minimum voltage of the output signal of the level shifter 12, and both the detector circuits 16 and 17 from the node of two resistance R_3 of the same resistance by which the series connection was carried out mutually, and R_4 .

[0033]The comparator 20 outputs high level, when the level of the output signal of the level shifter 12 inputted into one input terminal IN is larger than the predetermined reference voltage (henceforth threshold voltage) V_r applied to the input terminal REF of another side, and when small, it outputs the digital signal of a low level. This comparator 20 comprises a semiconductor device for ultrahigh frequency (for example, gallium arsenide type FET), etc.

[0034]The middle voltage V_o outputted from the intermediate voltage detector circuit 15 and the threshold voltage V_r are inputted into the control circuit 21 which is a control means of this waveform shaping circuit 10. The control circuit 21 detects the difference of the middle voltage V_o and the threshold voltage V_r which are inputted with the subtractor 22, and outputs the difference voltage signal to the level shifter 12 via the low pass filter 23, The middle voltage V_o controls the shift amount of the level shifter 12 in the direction which is in agreement with the threshold voltage V_r .

[0035]Drawing 3 shows an example of the more concrete circuit of the intermediate voltage detector circuit 15 and the control circuit 21.

[0036]Namely, the diode 16a by which the anode side was connected to the output of the level shifter 12 in the maximum detector circuit 16, It has the Masakata-oriented peak detection circuit formed by the capacitor 16b connected with the cathode of the diode 16a between groundings, Between the node of this diode 16a and capacitor 16b, and predetermined negative supply- V_1 , the constant current source 16c which sends very small forward bias current is connected to the diode 16a.

[0037]The diode 17a by which the cathode side was connected to the output of the level shifter

12 in the minimum value detecting circuit 17, It has a peak detection circuit of the negative direction formed by the capacitor 17b connected between the anode side of the diode 17a, and grounding, Between the node of the diode 17a and the capacitor 17b, and predetermined positive supply $+V_1$, the constant current source 17c which sends very small forward bias current is connected to the diode 17a.

[0038]Therefore, from the node of the diode 16a of the maximum detector circuit 16, and the capacitor 16b, The high-level voltage more than negative supply- V_1 voltage will be outputted among the digital signals outputted from the level shifter 12, and the low-level voltage below positive supply $+V_1$ voltage will be outputted from the node of the diode 17a of the minimum value detecting circuit 17, and the capacitor 17b.

[0039]The forward bias current from the constant current sources 16c and 17c over each diodes 16a and 17a hardly affects it to an input digital signal, but is set as the current value about [required to compensate the nonlinearity of detection operation of each diodes 16a and 17a moreover] 1microA.

[0040]The capacity value of the capacitors 16c and 17c is set as the value of about 1000 PF which can hold the peak value of the digital signal of 1 kHz or more of cycle periods in consideration of the forward bias current over each diodes 16a and 17a being a 1microA grade.

[0041]The subtractor 22 of the control circuit 21 is formed of the differential amplifier 22a and the feedback resistor 22b, and the voltage according to the difference of the intermediate voltage V_o and the threshold voltage V_r is outputted from the differential amplifier 22a. The low pass filter 23 formed by the resistance 23a and the capacitor 23b outputs the error signal V_e excluding the noise component from the output of the differential amplifier 22a to the level shifter 12.

[0042]Therefore, since the output voltage of the differential amplifier 22a will rise if the middle voltage V_o falls to the threshold voltage V_r , the level of the digital signal which the error signal V_e goes up and is outputted from the level shifter 12 goes up to the whole. Conversely, since the output voltage of the differential amplifier 22a will decline if the middle voltage V_o rises to the threshold voltage V_r , the level of the digital signal which the error signal V_e falls and is outputted from a level shifter will fall to the whole.

[0043]Next, operation of the above-mentioned waveform shaping circuit 10 is explained.

[0044]Now, temporarily, the maximum of the digital signal inputted to the level shifter 12 by time t_0 and the mean value of the minimum presuppose that it is equal to the threshold voltage V_r of the comparator 20, as shown in (a) of drawing 4.

[0045]In this case, since the output of the subtractor 22 of the control circuit 21 serves as zero, the digital signal inputted into the level shifter 12 is inputted into the comparator 20 as it is, and waveform shaping is carried out on the threshold voltage V_r .

[0046]And in time t_1 , as shown in (a) of drawing 4, the direct current offset voltage of the digital signal inputted presupposes that it went up to step form. As the output signal of the level shifter 12 is also shown in (b) of the figure according to this, an ascending change is carried out, and as the output voltage of the minimum value detecting circuit 17 in the maximum detector circuit 16 of the intermediate voltage detector circuit 15 is also shown in (c) of the figure, and (d), it changes to step form.

[0047]For this reason, as the middle voltage V_o to the subtractor 22 is also shown in (e) of the figure, it changes to step form, and the output of the subtractor 22 changes in the minus direction a lot, as shown in (f) of the figure.

[0048]Therefore, from the low pass filter 23, as shown in (g) of the figure, the error signal V_e which descends at the speed according to the damping time constant is outputted.

[0049]For this reason, since the shift amount of the level shifter 12 also increases to the minus side at ****, the mean value of the digital signal inputted into the comparator 20 changes in the direction which is in agreement with the threshold voltage V_r , as shown in (b) of the figure.

[0050]As a result, in time t_2 , the difference between the input voltage of the subtractor 22 is set to about 0, this stable state is continued henceforth, and the digital signal by which waveform shaping was carried out certainly is acquired from the output of the comparator 20.

[0051]Henceforth, even if offset of an input digital signal changes, since feedback control is always carried out in the direction approaching the threshold voltage V_r , positive waveform-shaping operation stabilizes for it and continues the middle voltage of the digital signal inputted into a comparator.

[0052]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1]It is a block diagram showing the 1st example composition of this invention.

[Drawing 2]It is a circuit diagram showing an example of the concrete circuit of the important section of drawing 1.

[Drawing 3]It is a circuit diagram showing an example of the concrete circuit of the important section of drawing 1.

[Drawing 4]It is a signal figure for explaining operation of one example.

[Drawing 5]It is a block diagram showing the composition of the 2nd example of this invention.

[Drawing 6]It is a circuit diagram showing the modification of the important section of the 2nd example.

[Drawing 7]It is a circuit diagram showing the modification of the important section of the 2nd example.

[Drawing 8]It is a circuit diagram showing the modification of the important section of the 2nd example.

[Drawing 9]It is a circuit diagram showing the modification of the important section of the 1st and 2nd example.

[Drawing 10]It is a circuit diagram for reading a shift amount directly.

[Drawing 11]It is a block diagram showing the composition of the 3rd example of this invention.

[Drawing 12]It is a figure for explaining operation of the 3rd example.

[Drawing 13]It is an important section block diagram showing the modification of the 3rd example.

[Drawing 14]It is a block diagram showing other modifications of the 3rd example.

[Drawing 15]It is a block diagram showing other modifications of the 3rd example.

[Drawing 16]It is a block diagram showing the important section of the 3rd example more concretely.

[Drawing 17]It is a block diagram showing the composition of a device conventionally.

[Drawing 18]It is a signal figure for explaining operation of a device conventionally.

[Description of Notations]

10 10' Waveform shaping circuit

12 Level shifter

15 Intermediate voltage detector circuit

16 Maximum detector circuit

17 Minimum value detecting circuit
18 Intermediate voltage output circuit
20 Comparator
21 Control circuit
22 Subtractor
23 Low pass filter
25 Hold circuit
26 and 27 Switch
29 Stop circuit
32 A/D converter
33 Memory circuit
34 D/A converter
35 Switch
37 Voltmeter
50 Waveform shaping circuit
52 Level shifter
55 Intermediate voltage detector circuit
60 Comparator
61 The 1st control circuit
65 A/D converter
71 Variable delay device
72 Discrimination circuit
75 Error test section
76 Criterion data generator
77 Code comparison machine
78 Inharmonious counter
79 Clock counter
80 Control section
81 Display for indication
90 Operation control part
101 Waveform shaping circuit
102 Variable delay device
103 Discrimination circuit
104 1/N demultiplexer
105 Timing generation part
106 Error detection part
107 an error -- calculation -- a part
108 Indicator
109 Synchronous controlling part
110 Reference pattern generating part
111 CPU
112 Auto search part

[Translation done.]

(19)日本国特許庁 (J P)

(12) 公 開 特 許 公 報 (A)

(11)特許出願公開番号

特開平5-7135

(43)公開日 平成 5 年(1993) 1 月14日

(51)Int.Cl.⁵

H 0 3 K 5/08

識別記号

庁内整理番号

R 7125-5 J

F I

技術表示箇所

審査請求 未請求 請求項の数 3 (全 20 頁)

(21)出願番号 特願平3-270188

(22)出願日 平成 3 年(1991) 9 月21日

(31)優先権主張番号 特願平2-261875

(32)優先日 平 2 (1990) 9 月29日

(33)優先権主張国 日本 (J P)

(31)優先権主張番号 特願平2-261876

(32)優先日 平 2 (1990) 9 月29日

(33)優先権主張国 日本 (J P)

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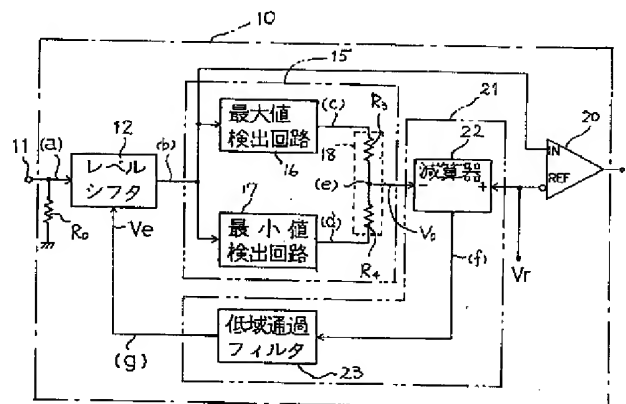
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(54)【発明の名称】 波形整形回路およびデジタル信号解析装置

(57)【要約】

【目的】 入力されるデジタル信号を、その振幅変化やオフセットの影響を受けずに安定に波形整形する。

【構成】 入力されるデジタル信号は、レベルシフタ 12 を介して中間電圧検出回路 15 へ入力される。中間電圧検出回路 15 は、入力されたデジタル信号のハイレベルとローレベルとの中間の電圧 V_0 を検出して、制御回路 21 の減算器 22 へ出力する。制御回路 21 は、中間の電圧 V_0 と参照電圧 V_r との差信号を、低域通過フィルタ 23 を介してレベルシフタ 12 へ出力し、中間の電圧 V_0 が参照電圧 V_r に近づく方向にレベルシフタ 12 のシフト量を制御する。レベルシフタ 12 によってレベルシフトされたデジタル信号は、参照電圧 V_r をしきい値とするコンパレータ 20 へ入力されて波形整形される。



【特許請求の範囲】

【請求項1】入力されたデジタル信号の直流オフセット電圧を可変制御するレベルシフタ(12)と、該レベルシフタから出力されたデジタル信号を所定の参照電圧と比較し、波形整形して出力するコンパレータ(20)と、前記レベルシフタから出力されたデジタル信号のハイレベル電圧とローレベル電圧との中間の電圧を検出して出力する中間電圧検出手段(15)と、該中間電圧検出手段から出力される中間の電圧と前記所定の参照電圧とを受けて、前記中間の電圧を前記所定の参照電圧と等しくするために前記直流オフセット電圧を変化させる制御信号を前記レベルシフタに出力する制御手段(21)とを備えた波形整形回路。

【請求項2】前記制御手段から出力された前記制御信号を保持する保持手段(25)と、該保持手段によって前記制御信号が保持されたとき、前記中間電圧検出手段の作動を停止させる停止手段(26)、(27)とを備えた第1項記載の波形整形回路。

【請求項3】入力されたデジタル信号の直流オフセット電圧を可変制御するレベルシフタ(52)と、該レベルシフタから出力されたデジタル信号を所定の参照電圧と比較し、波形整形して出力するコンパレータ(60)と、前記レベルシフタから出力されたデジタル信号のハイレベル電圧とローレベル電圧との中間の電圧を検出して出力する中間電圧検出回路(55)と、該中間電圧検出回路から出力される中間の電圧と前記所定の参照電圧とを受けて、前記中間の電圧を前記所定の参照電圧と等しくするために前記直流オフセット電圧を変化させる制御信号を前記レベルシフタに出力する第1の制御手段(61)と、入力されたクロック信号と前記コンパレータの出力との間の位相を相対的に可変する可変遅延器(71)と、該可変遅延器によって位相が相対的に可変された、前記コンパレータの出力と前記クロック信号とを受けて、該クロック信号の立上りまたは立下り時における前記コンパレータの出力信号の符号を判定する識別器(72)と、該識別器からの判定信号と前記入力されたデジタル信号に相当する基準信号とを比較して誤り信号を出力する誤り測定器(75)と、該誤り測定器の出力を受けて相隣り合って誤り信号が最大値となる遅延量のほぼ中間の遅延量を検出して、かつ、この中間遅延量を前記可変遅延器に送出して前記誤り測定器が出力する前記誤り信号を減少させる第2の制御手段(80)とを備えたデジタル信号解析装置。

【発明の詳細な説明】**【0001】**

【産業上の利用分野】本発明は、入力されるデジタル信号を波形整形して出力する波形整形回路および、ロジックアナライザや誤り測定装置などのようにクロック信号に同期して入力されるデジタル信号を解析するデジタル信号解析装置に関する。

【0002】

【従来の技術と解決しようとする課題】一般に、前述したロジックアナライザや誤り測定装置等のデジタル信号解析装置では、外部から入力されるデジタル信号を、コンパレータで構成される波形整形回路によって波形整形した後、その2値判定を行なうよう構成されている。

【0003】この種の波形整形回路では、コンパレータの動作点を、入力されるデジタル信号のオフセットに対応し、且つノイズの影響を受けない最良の動作点に設定する必要がある。この動作点を設定するために、従来は、次の3つの方法のいずれかを実施していた。

【0004】(1)コンパレータの出力波形をモニタしながらコンパレータに対するしきい値レベル(参照電圧)を手動で最適状態に設定する手法。

【0005】(2)入力されるデジタル信号をコンデンサを介してコンパレータに入力させてオフセットの影響を除く手法。

【0006】(3)入力されるデジタル信号の直流平均レベルを予め想定してレベルシフタで手動可変してコンパレータに入力する手法。

【0007】しかしながら、前述した(1)、(3)の手法では、手動による動作点設定が煩しく、入力信号のレベルやオフセットが変わる毎にその設定動作を行わなければならない。

【0008】また、前述した(2)の手法では、入力されるデジタル信号のマーク率(発生する全ビット数とその中に含まれるマーク数との比)に応じてコンパレータに入力されるデジタル信号のオフセット電圧が変化してしまい、固定したしきい値で、確実な波形整形が行えない。

【0009】このため、入力されるデジタル信号のハイレベル電圧とローレベル電圧の中間電圧をしきい値としてコンパレータに入力する手法も考えられる。

【0010】ところが、この手法は、同相入力範囲の広い比較的低速のコンパレータの場合に有効であるが、超高周波(数GHz)の信号を波形整形するためのコンパレータのように、同相入力範囲が極めて狭い場合には、入力信号のオフセット電圧の変化によってコンパレータ自身が飽和してしまい、正常な波形整形動作が行えないという問題がある。

【0011】一方、波形整形したデジタル信号の2値判定を行なって、そのデジタルデータを解析するデジタル信号解析装置は、従来から図17に示すように構成されている。

【0012】即ち、一方の入力端子1に入力される被測定データ信号は、参照電圧発生器2からの参照電圧 V_r をしきい値とするコンパレータ3によって波形整形される。この参照電圧 V_r は、前述した手法のいずれかによって予め最良の値に設定されているため、図18の

(a) に示す被測定データ信号の振幅方向のゆらぎ成分は、同図の(b) に示すように波形整形されて、Dタイプのフリップフロップで構成された識別器4のデータ入力端子Dに入力される。

【0013】また、他方の入力端子5に入力されるクロック信号は可変遅延器6を介して、識別器4のクロック端子CPへ入力される。

【0014】この可変遅延器6は、識別器4に入力されるデータ信号の2値レベルが、最も安定しているタイミングにクロック信号が立上がるように、予め調整されている。

【0015】この調整として、図18の(b) に示したコンパレータ3の出力信号と、同図の(c) に示すクロック信号とを2現象オシロスコープに表示して、クロック信号の立上がりタイミングが、デジタル信号の状態遷移点I、IIのほぼ中間点(位相余裕が最も大きい点)に位置するように、可変遅延器6の遅延量を手動により調整する方法が従来よりとられていた。

【0016】このようにして、コンパレータ3からのデジタル信号は、識別器4に入力されるクロック信号の立上りタイミングで2値の識別がなされ、その判定出力は、クロック信号とともにデータ解析部7へ入力されて、所定のデータ解析がなされる。

【0017】しかしながら、このような構成の従来のデジタル信号解析装置では、前述した波形整形回路の手動調整に加えて、遅延量の手動調整も行なわなければならないが、操作者の個人差によってこれらの設定量の差が生じやすく、解析結果にも差がでてしまうという問題があった。

【0018】また、オシロスコープで波形観測して調整を行なう場合、機器間の接続が煩雑であるばかりでなく、オシロスコープの接続によって信号の波形が乱れ、誤動作を引き起こすことがある。特に、前述したように超高周波(数GHz)の信号に波形観測用のケーブルを接続する場合には、この波形の乱れが大きく正確な調整が困難となる。

【0019】このため、デジタル信号解析装置に波形観測用のモニタ端子を設ける手法もあるが、オシロスコープ等の波形観測用機器を常時準備しておかなければならないことになり、非常に不便であった。

【0020】本発明は、前述した問題を解決した波形整形回路およびデジタル信号解析装置を提供することを目的としている。

【0021】

【課題を解決するための手段】前記課題を解決するために、本発明の波形整形回路は、入力されたデジタル信号の直流オフセット電圧を可変制御するレベルシフタ(12)と、該レベルシフタから出力されたデジタル信号を所定の参照電圧と比較し、波形整形して出力するコンパレータ(20)と、前記レベルシフタから出力さ

れたデジタル信号のハイレベル電圧とローレベル電圧との中間の電圧を検出して出力する中間電圧検出手段

(15)と、該中間電圧検出手段から出力される中間の電圧と前記所定の参照電圧とを受けて、前記中間の電圧を前記所定の参照電圧と等しくするために前記直流オフセット電圧を変化させる制御信号を前記レベルシフタに出力する制御手段(21)とを備えている。

【0022】また、本発明のデジタル信号解析装置は、入力されたデジタル信号の直流オフセット電圧を可変制御するレベルシフタ(52)と、該レベルシフタから出力されたデジタル信号を所定の参照電圧と比較し、波形整形して出力するコンパレータ(60)と、前記レベルシフタから出力されたデジタル信号のハイレベル電圧とローレベル電圧との中間の電圧を検出して出力する中間電圧検出回路(55)と、該中間電圧検出回路から出力される中間の電圧と前記所定の参照電圧とを受けて、前記中間の電圧を前記所定の参照電圧と等しくするために前記直流オフセット電圧を変化させる制御信号を前記レベルシフタに出力する第1の制御手段(61)と、入力されたクロック信号と前記コンパレータの出力との間の位相を相対的に可変する可変遅延器(71)と、該可変遅延器によって位相が相対的に可変された、前記コンパレータの出力と前記クロック信号とを受けて、該クロック信号の立上りまたは立下り時における前記コンパレータの出力信号の符号を判定する識別器(72)と、該識別器からの判定信号と前記入力されたデジタル信号に相当する基準信号とを比較して誤り信号を出力する誤り測定器(75)と、該誤り測定器の出力を受けて相隣り合って誤り信号が最大値となる遅延量のほぼ中間の遅延量を検出して、かつ、この中間遅延量を前記可変遅延器に送出して前記誤り測定器が出力する前記誤り信号を減少させる第2の制御手段(80)とを備えている。

【0023】

【作用】このように構成されているため、本発明の波形整形回路では、入力されるデジタル信号は、レベルシフタを介してコンパレータに入力され、所定の参照電圧によって波形整形される。また、レベルシフタから出力されるデジタル信号のハイレベル電圧とローレベル電圧の中間の電圧は、中間電圧検出手段によって検出されて、参照電圧とともに制御手段へ出力される。制御手段は、中間の電圧が参照電圧と等しくなるための制御信号をレベルシフタに出力して、入力されるデジタル信号の直流オフセット電圧を可変する。

【0024】また、本発明のデジタル信号解析装置では、上記発明の波形整形回路と同一構成の波形整形回路によって波形整形されたコンパレータの出力信号と入力端子から入力されたクロック信号とは、その間の位相が可変遅延器によって可変されて、識別器に入力される。識別器からの判定信号は、誤り測定器によって、入力さ

れたデジタル信号に相当する基準信号と比較される。誤り測定器によって検出された誤り信号は、第2の制御手段に入力される。第2の制御手段は、誤り測定器からの誤り信号を受けながら、可変遅延器の遅延量を可変し、相隣り合って誤り信号が最大となる遅延量のほぼ中間遅延量を検出して、可変遅延器に出力する。

【0025】

【実施例】以下、図面に基づいて本発明の第1実施例を説明する。

【0026】図1は、第1の実施例の波形整形回路10の構成を示す回路図である。

【0027】図1において、端子11に入力される入力デジタル信号は、入力抵抗 R_0 （例えば 50Ω ）で終端され、レベルシフタ12に入力される。

【0028】レベルシフタ12は、入力デジタル信号の平均直流（オフセット）電圧レベルを、後述する制御回路21からの誤差信号（制御信号） V_e の大きさに応じて可変する。このために、レベルシフタ12は、例えば図2に示すように構成されている。

【0029】即ち、入力デジタル信号の平均直流電圧は、抵抗 R_1 とコンデンサ C_1 による積分回路で検出され、加算器13に入力される。加算器13は、誤差信号 V_e をこの平均直流電圧に加算し、その加算電圧を、抵抗 R_2 を介して出力する。抵抗 R_2 と端子11との間には、入力デジタル信号の交流成分のみを通過させるコンデンサ C_2 が設けられている。したがって、コンデンサ C_2 と抵抗 R_2 との接続点からは、入力デジタル信号の交流成分に加算器13からの出力電圧が加えられた信号、即ち、入力デジタル信号に対して誤差電圧 V_e だけレベルがシフトされた信号が出力される。

【0030】なお、抵抗 R_1 、 R_2 は、 50Ω の伝送インピーダンスに影響のない数 $10K\Omega$ 程度の高抵抗値を有する。

【0031】レベルシフタ12の出力は、図1に示すように、中間電圧検出回路15および後述するコンパレータ20へ入力されている。

【0032】中間電圧検出回路15は、レベルシフタ12の出力信号の最大電圧を検出する最大値検出回路16と、レベルシフタ12の出力信号の最小電圧を検出する最小値検出回路17と、両検出回路16、17の出力電圧間の中間の電圧を、互いに直列接続された同一抵抗値の2つの抵抗 R_3 、 R_4 の接続点から出力する中間電圧出力回路18によって構成されている。

【0033】コンパレータ20は、一方の入力端子INに入力されるレベルシフタ12の出力信号のレベルが、他方の入力端子REFに加えられる所定の参照電圧（以下しきい値電圧ともいう） V_r より大きいときにハイレベル、小さいときにローレベルのデジタル信号を出力する。このコンパレータ20は、超高周波用の半導体素子（例えばガリウムヒ素型FET）等で構成されてい

る。

【0034】中間電圧検出回路15から出力される中間の電圧 V_o と、しきい値電圧 V_r は、この波形整形回路10の制御手段である制御回路21に入力されている。制御回路21は、入力される中間の電圧 V_o としきい値電圧 V_r との差を減算器22によって検出し、その差電圧信号を低域通過フィルタ23を介してレベルシフタ12に出力して、中間の電圧 V_o がしきい値電圧 V_r に一致する方向にレベルシフタ12のシフト量を制御する。

【0035】図3は、中間電圧検出回路15および制御回路21のより具体的な回路の一例を示している。

【0036】即ち、最大値検出回路16は、レベルシフタ12の出力にアノード側を接続されたダイオード16aと、ダイオード16aのカソードと接地間に接続されたコンデンサ16bとによって形成された正方向のピーク検波回路を有し、このダイオード16aとコンデンサ16bとの接続点と所定の負電源 $-V_1$ の間には、ダイオード16aに微少の順方向バイアス電流を流す定電流源16cが接続されている。

【0037】また、最小値検出回路17は、レベルシフタ12の出力にカソード側を接続されたダイオード17aと、ダイオード17aのアノード側と接地間に接続されたコンデンサ17bとによって形成された負方向のピーク検波回路を有し、ダイオード17aとコンデンサ17bとの接続点と所定の正電源 $+V_1$ の間には、ダイオード17aに微少の順方向バイアス電流を流す定電流源17cが接続されている。

【0038】したがって、最大値検出回路16のダイオード16aとコンデンサ16bとの接続点からは、レベルシフタ12から出力されるデジタル信号のうち、負電源 $-V_1$ 電圧以上のハイレベル電圧が出力され、最小値検出回路17のダイオード17aとコンデンサ17bとの接続点からは、正電源 $+V_1$ 電圧以下のローレベル電圧が出力されることになる。

【0039】各ダイオード16a、17aに対する定電流源16c、17cからの順方向バイアス電流は、入力デジタル信号に対してほとんど影響を与えず、しかも各ダイオード16a、17aの検波動作の非直線性を補償するのに必要な $1\mu A$ 程度の電流値に設定されている。

【0040】なお、コンデンサ16c、17cの容量値は、各ダイオード16a、17aに対する順方向バイアス電流が $1\mu A$ 程度であることを考慮して、繰返し周期 $1KHz$ 以上のデジタル信号のピーク値をホールドできる $1000PF$ 程度の値に設定されている。

【0041】制御回路21の減算器22は、差動増幅器22aと帰還抵抗22bによって形成され、中間電圧 V_o としきい値電圧 V_r との差に応じた電圧が差動増幅器22aから出力される。抵抗23aとコンデンサ23bで形成された低域通過フィルタ23は、差動増幅器22

aの出力から雑音成分を除いた誤差信号 V_e をレベルシフタ12へ出力する。

【0042】したがって、中間の電圧 V_o がしきい値電圧 V_r に対して低下すると、差動増幅器22aの出力電圧は上昇するため、誤差信号 V_e が上昇してレベルシフタ12から出力されるデジタル信号のレベルが全体に上昇する。逆に中間の電圧 V_o がしきい値電圧 V_r に対して上昇すると、差動増幅器22aの出力電圧は低下するため、誤差信号 V_e が低下してレベルシフタから出力されるデジタル信号のレベルが全体に低下することになる。

【0043】次に、上記の波形整形回路10の動作を説明する。

【0044】今、仮に、時刻 t_0 で、レベルシフタ12に対して入力されるデジタル信号の最大値と最小値の中間値が、図4の(a)に示すようにコンパレータ20のしきい値電圧 V_r に等しいとする。

【0045】この場合、制御回路21の減算器22の出力は零となるので、レベルシフタ12に入力されるデジタル信号は、そのままコンパレータ20に入力され、しきい値電圧 V_r で波形整形される。

【0046】そして時刻 t_1 において、図4の(a)に示すように、入力されるデジタル信号の直流オフセット電圧がステップ状に上昇したとする。これに応じてレベルシフタ12の出力信号も同図の(b)に示すように上昇変化し、中間電圧検出回路15の最大値検出回路16、最小値検出回路17の出力電圧も同図の(c)、(d)に示すようにステップ状に変化する。

【0047】このため、減算器22への中間の電圧 V_o も同図の(e)に示すようにステップ状に変化し、減算器22の出力は、同図の(f)に示すようにマイナス方向に大きく変化する。

【0048】したがって、低域通過フィルタ23からは、同図の(g)に示すように、その時定数に応じた速度で下降する誤差信号 V_e が出力される。

【0049】このため、レベルシフタ12のシフト量もマイナス側に徐々に増加するので、コンパレータ20に入力されるデジタル信号の中間値は、同図の(b)に示すように、しきい値電圧 V_r に一致する方向に変化する。

【0050】この結果、時刻 t_2 においては、減算器22の入力電圧間の差はほぼ零となり、以降は、この安定状態が継続され、確実に波形整形されたデジタル信号がコンパレータ20の出力から得られる。

【0051】以後、入力デジタル信号のオフセットが変化しても、コンパレータへ入力されるデジタル信号の中間の電圧は、しきい値電圧 V_r に近づく方向に常にフィードバック制御されるため、確実な波形整形動作が安定して継続する。

【0052】

【第2の実施例】なお、前記第1の実施例では、レベルシフタ12のシフト量を制御するための制御ループを常に閉じていたが、入力デジタル信号に対するシフト量が安定して適正量になった後、このシフト量をホールドしてループを開くとともに、信号ラインに接続されている中間電圧検出回路15の検波動作を停止させるように構成することもできる。

【0053】図5は、第2の実施例であるこのホールド型の波形整形回路10'の構成を示している。この波形整形回路10'は、ホールド信号(停止信号)を受けて誤差信号の大きさを保持するホールド回路25と、ホールド信号(停止信号)によって閉じて最大値検出回路16、最小値検出回路17のダイオード16a、17aに逆バイアス電圧 $\pm V_2$ を与えるスイッチ26、27(停止手段)とを有している。

【0054】このように構成された波形整形回路10'では、入力デジタル信号に対するレベルシフタ12のシフト量が、前記同様のループ制御によって適正量になった後に、ホールド信号(停止信号)を入力すると、適正なシフト量を与える誤差信号 V_e の値がホールド回路25にホールドされて、レベルシフタ12のシフト量が適正量に固定される。また、このとき、中間電圧検出回路15の両検出回路16、17のダイオード16a、17aは、逆バイアス電圧によってデジタル信号のラインから電気的に切離されるため、このラインに対するダイオード接続の悪影響(高周波特性の悪化)を防ぐことができる。

【0055】なお、図5に示した波形整形回路10'では、ホールド信号によって、逆方向バイアス電圧 $\pm V_2$ を最大値検出回路16と最小値検出回路17に単に印加する場合について説明したが、図3に具体例を示した中間電圧検出回路15のように、ダイオード16a、17aに対して定電流源16c、17cから順方向の微小電流を加えている場合には、この定電流源と逆バイアス電圧 $\pm V_2$ との切換えを、ホールド信号によって行なうようにしてもよい。

【0056】図6は、定電流源16c、17cと逆バイアス電圧 $\pm V_2$ とを切換えることによって、中間電圧検出回路15の検波動作を停止させる停止回路29の具体的な回路構成を示している。

【0057】この停止回路29は、前述のホールド信号を停止信号として受けて、スイッチ26'、27'をノーマルモードからホールド/リミッタモードへ切換える。ノーマルモードにおいて、ダイオード16a、17aには、前記同様に微小な順方向バイアス電流が定電流源16c、17cから供給されるため、中間電圧検出回路15は、レベルシフタ12からのデジタル信号の最大値、最小値の検出を行なう。

【0058】ホールドモードにおいては、入力デジタル信号の最大、最小値よりも十分に大きい(例えば、4

ボルト程度)逆バイアス電圧 $\pm V_2$ が、ダイオード16a、17aに加えられるため、中間電圧検出回路15は、最大値、最小値の検出動作を停止する。

【0059】リミットモードにおいては、ダイオード16a、17aの順方向電圧降下分0.7ボルトを見込んだ1.3ボルト程度の逆バイアス電圧 $\pm V_2$ がダイオード16a、17aに加えられるため、入力デジタル信号に対してほぼ $\pm 2V$ でリミットをかけることができる。

【0060】以上のように、図6の回路では、逆バイアス電圧 $\pm V_2$ として設定する電圧を、そのときの状態に応じて4ボルトまたは1.3ボルトになるように可変制御することにより、ホールドモードまたはリミットモードの両方を上述のノーマルモードと共に切換えて使用することができる。なお、図6において、符号16d、17dはそれぞれバッファアンプである。

【0061】また、停止回路29を図7に示すように構成すれば、前述のノーマルモードおよびホールドモードのいずれの場合でもダイオード16a、17aをリミット動作させることが可能となる。

【0062】図7に示した停止回路29では、ダイオード16a、17aに対して常に0.6ボルト程度の逆バイアス電圧 $\pm V_3$ がダイオード30、31を介して印加されている。また、最大値検出回路16側のスイッチ26'のホールド側には、最小値検出回路17側の定電流源17cが接続され、最小値検出回路17側のスイッチ27'のホールド側には、最大値検出回路16側の定電流源16cが接続されている。

【0063】このため、ノーマルモード時において、ダイオード16a、17aにそれぞれの定電流源16c、17cからの順方向バイアスがかけられて、入力デジタル信号に対する最大値、最小値検出が行なわれることは前記図6の回路の場合と同様である。

【0064】しかるに、このノーマルモードにおいて、レベルシフタ12からの出力電圧が $-2V$ よりも低くなると、最小値検出回路17のダイオード17aおよびダイオード31が導通するため最小値検出回路17側は $-2V$ ($-V_3 - 1.4V$)でリミットがかかることになる。

【0065】また、ノーマルモードにおいて、レベルシフタ12からの出力電圧が $+2V$ よりも高くなると、最大値検出回路16側のダイオード16aおよびダイオード30が導通するため、最大値検出回路16側は $+2V$ ($+V_3 + 1.4V$)でリミットがかかることになる。

【0066】なお、以上において、 $-1.4V$ はダイオード17a、31での電圧降下分であり、 $+1.4V$ はダイオード16a、30での電圧降下分である。

【0067】また、ホールドモード時において、ダイオード16a、17aは、それぞれ定電流源17c、16c側からの逆バイアスによって、入力デジタル信号に

対する最大値、最小値検出動作が停止される。

【0068】しかるに、このホールドモードにおいて、 $\pm V_1 = \pm 1.3V$ 程度に設定しておけば、レベルシフタ12からの出力電圧が $-2V$ よりも低くなるかあるいは $+2V$ よりも高くなると、それぞれ上述したノーマルモード時と同様に $-2V$ または $+2V$ でリミットがかかるようになる。

【0069】なお、前記した図5、図6、図7のホールド回路25としては、アナログ型のホールド回路の他に図8に示すように、デジタル型のホールド回路を用いることもできる。

【0070】図8に示したホールド回路25は、制御回路21からの誤差信号 V_e をA/D変換器32でデジタル値に変換し、ホールド信号(切換信号)が入力されたときのデジタル値をメモリ回路33に記憶する。メモリ回路33に記憶されたデジタル値は、D/A変換器34によってアナログ電圧に変換され、スイッチ35を介してレベルシフタ12へ出力される。

【0071】スイッチ回路35は、ホールド信号が入力されていないとき、制御回路21からの誤差信号をそのままレベルシフタ12へ出力し、ホールド信号が入力されているとき、D/A変換器34からの信号を出力する。このようなデジタル型のホールド回路は、アナログ型のホールド回路に比べて、ホールド出力の変動が無いため、長時間のホールド動作が必要となるときに有利である。

【0072】また、前記説明では制御回路21の具体的な回路として、減算器22と低域通過フィルタ23とを別構成にしていたが、図9に示すように、演算増幅器21aの出力をコンデンサ21bによって帰還する積分型の回路を用いて制御回路を簡単化することもできる。

【0073】また、前記実施例において、レベルシフタ12におけるシフト量を知りたい場合には、誤差信号 V_e の大きさを電圧計で読んだり、図10に示すように、抵抗 R_5 とコンデンサ C_5 の積分回路でそれぞれ検出されたレベルシフタ12の入出力間の平均直流電圧の差を、電圧計37で読むようにすれば、レベルシフタ12のシフト量を知ることができる。また、このレベルシフト量から入力デジタル信号のスレッシュホールドレベルを知ることができる。なお、図8に示したデジタル型のホールド回路25を用いた場合、A/D変換器32によってレベルシフタ12におけるシフト量を検知できるので、図10のような回路は不要である。

【0074】また、前記実施例は、超高周波で使用される波形整形回路について説明したが、本発明の波形整形回路は、低い周波数帯の波形整形回路にも適用することができる。

【0075】さらに、コンパレータとしては、前記実施例のガリウムヒ素型のFETで構成されたものだけでなく、例えば、シリコンバイポーラトランジスタやヘテ

ロバイポーラトランジスタ(HBT)で構成されたコンパレータを用いてもよい。また、レベルシフトについても前記実施例の構成の他に、直流阻止コンデンサと高周波阻止コイルで構成されたレベルシフト等種々のものが使用できる。

【0076】

【第3の実施例】次に、以上のような波形整形回路を用いるデジタル信号解析装置について説明する。

【0077】図11は、第3の実施例として、本発明のデジタル信号解析装置を誤り測定装置に適用した場合の構成を示すブロック図である。

【0078】この誤り測定装置は、クロック信号とともに入力される被測定データ信号を波形整形した後、その2値判定を、入力されたクロック信号に同期したタイミングで識別し、識別された信号を入力されたデジタル信号に相当する基準信号のデータと比較するように構成されている。

【0079】被測定データ信号は、前述した図1の波形整形回路10と同一構成の波形整形回路50に入力される。

【0080】即ち、入力端子51から入力された被測定データ信号は、入力抵抗 R_0 （例えば50Ω）で終端され、レベルシフト52に入力される。レベルシフト52は、入力された被測定データ信号の直流平均（オフセット）電圧を、誤差信号 V_e の大きさに応じて可変する。

【0081】レベルシフト52の出力は、中間電圧検出回路55およびコンパレータ60に入力される。中間電圧検出回路55は、レベルシフト52から出力されるデジタル信号のハイレベルのピーク電圧とローレベルのピーク電圧を、ハイレベルピーク検出回路（最大値検出回路）56とローレベルピーク検出回路（最小値検出回路）57でそれぞれ検出し、その中間の電圧 V_o を、等しい2つの抵抗 R の中点から出力する。

【0082】この中間の電圧 V_o は、参照電圧発生器59からの参照電圧（しきい値電圧） V_r とともに第1の制御回路61に入力される。

【0083】第1の制御手段である第1の制御回路61は、参照電圧 V_r と中間の電圧 V_o との差を検出する減算回路62と、減算回路62の減算出力を積分して得た誤差信号 V_e を出力する低域通過フィルタ（以下、LPFと記す）63で構成され、中間の電圧 V_o が常に参照電圧 V_r に近づく方向にレベルシフト52のシフト量をフィードバック制御する。

【0084】コンパレータ60は、レベルシフト52から出力されるデジタル信号が、参照電圧 V_r より高いときハイレベル、低いときローレベルのデジタル信号を出力して、入力されたデジタル信号を波形整形する。

【0085】以上の構成は、前述したように、図1に示した波形整形回路10と全く同一であり、各部の詳細お

よび変形例については、前述の説明によるものとする。

【0086】一方、入力端子70に入力されたクロック信号は可変遅延器71を介して、識別器72および誤り測定器である誤り測定部75へ入力されている。可変遅延器71は、入力されるクロック信号を制御信号に応じて遅延し、被測定データ信号に対するクロック信号の位相を相対的に可変する。この可変遅延器71としては、信号線路長をスラグ可変することによって、その遅延量を可変する可変長スラブライン構造のものが、超高周波用として用いられる。

【0087】識別器72は、コンパレータ60から出力されるデジタル信号のレベルを、可変遅延器71から入力されるクロック信号の立上り（または立下がり）のタイミングで2値判定し、その識別出力を、誤り測定部75へ出力する。

【0088】この実施例による誤り測定装置のデータ解析部である誤り測定部75は、基準データ発生器76、符号比較器77、不一致カウンタ78およびクロックカウンタ79によって構成されている。

【0089】基準データ発生器76は、測定しようとするデータと同一パターンの基準データを、可変遅延器71からのクロック信号に同期したタイミングで符号比較器77へ出力する。

【0090】符号比較器77は、識別器72の出力と基準データとの符号の一致、不一致を判定し、不一致の場合には、不一致信号を不一致カウンタ78へ出力する。

【0091】不一致カウンタ78は、後述する制御部80からのゲート信号を受けている間、不一致信号の計数を継続して行なう。クロックカウンタ79は、制御部80からのゲート信号を受けている間、可変遅延器71から出力されるクロック信号の計数を行なう。

【0092】この誤り測定装置の第2の制御手段である制御部80は、マイクロプロセッサ(CPU)等で構成され、主に2つの処理モードを有している。

【0093】即ち、第1の処理モードは、不一致カウンタ78とクロックカウンタ79を同時に所定時間計数させた後、両カウンタの計数結果を読み込んで、符号誤り率の演算を行ない、その結果を表示器81に表示させる通常の測定処理である。第2の処理モードは、測定処理の前に、可変遅延器71のクロック信号に対する遅延量を所定範囲連続的に可変して、その遅延量に対する誤り率データを求め、メモリ80aに記憶して、誤り率が最小となる遅延量を検出する最適遅延量検出処理である。

【0094】なお、図11中のA/D変換器65は、波形整形回路50の第1の制御回路61からの誤差信号 V_e をデジタル値に変換し、この値をレベルシフト52のシフト量として制御部80へ出力する。制御部80は、このシフト量をメモリ80aに記憶したり、表示器81に表示させる。

【0095】次に、この誤り測定装置の動作について説

明する。

【0096】入力端子51、70に、それぞれ被測定データ信号とクロック信号が入力されると、波形整形回路50は、入力された被測定データ信号のハイレベルとローレベルの中間の電圧 V_o を参照電圧 V_r に一致させる方向に、シフト量を制御する。

【0097】この動作は、前述の図4によって説明した動作と全く同一である。

【0098】このため、コンパレータ60からは、図12の(a)に示すように、しきい値電圧(参照電圧) V_r で波形整形され、振幅方向にゆらぎのない被測定データ信号が出力される。

【0099】なお、レベルシフタ52のシフト量が安定したことは、A/D変換器65からのシフト量を表示器81に表示させるか、あるいは、制御部80自身でその安定判定処理を行なうことによって確認することができる。

【0100】次に、制御部80は前述した最適遅延量検出処理を行なう。

【0101】即ち、制御部80は、ゲート信号を所定時間クロックカウンタ79へ入力した後、その計数結果からクロック信号の周期 T を求める。そして、図12の(b_1)、(b_2)、(b_3)に示すように、可変遅延器71の遅延量を、初期値 D_0 から所定ステップ d で少なくともクロック信号の1周期分まで可変しながら、所定ステップ毎に誤り率を求め、その結果をメモリ80aに記憶する。

【0102】図12の(c)は、メモリ80aに記憶された遅延量の変化に対する誤り率の変化を示している。この図から明らかなように、位相成分にゆらぎのあるコンパレータ60の出力信号(同図の(a))に対し、同図の(b_1)から同図の(b_3)までクロック信号の立上りタイミングを1.5周期分可変したときの誤り率の変化は、コンパレータ60の出力信号の状態遷移点で最大となり、その最大点が2箇所得られる。

【0103】制御部80は、記憶した誤り率のデータに基づいて、例えば誤り率が最大となる遅延量 D_2 、 D_6 の中間値 D_4 を、最も位相余裕のある最適な遅延量として可変遅延器71に自動設定する。

【0104】以上の設定を行なった後、制御部80は、通常の誤り測定処理を行なって、測定された誤り率を順次表示器81に表示させる。

【0105】なお、A/D変換器65からのレベルシフト量や、このレベルシフト量とコンパレータ60への参照電圧 V_r から算出される被測定データ信号のスレッシュホールドレベルも表示器81に随時表示される。

【0106】また、この第3の実施例の誤り測定装置では、中間の電圧と参照電圧との減算結果をLPF63を介して、レベルシフタ52に入力していたが、図13に示すように、減算結果をA/D変換器65で減算データ

にデジタル変換し、この減算データが零に近づくためのシフト量を、演算制御部90によって算出し、この算出されたシフト量データをD/A変換器66に送出して、レベルシフタ52のシフト量を制御するように構成してもよい。なお、この演算制御部90は、制御部80とともに、1つのCPUに構成されている。

【0107】さらに、中間電圧検出回路55から出力される中間の電圧を直接A/D変換して、演算制御部90へ送り、演算制御部90によってこの中間電圧データを参照電圧データと比較して、その差に応じたシフト量データをD/A変換器65を介してレベルシフタ52に出力するように構成することも可能である。この場合には、演算制御部90が第1の制御手段となる。

【0108】また、前記第3の実施例では、クロック信号に対する最適な遅延量を設定するために、クロック信号の1周期分以上にわたって遅延量を可変して得られた誤り率の最大値から、最適値を決定していたが、誤り率が最小値となる遅延量をそのまま最適値として設定するようにしてもよい。これは、入力出信号の位相のゆらぎが大きく、図12の(c)の D_3 から D_5 の間の平坦部が極めて狭い場合に有効な方法である。

【0109】また、前記実施例のように最大の誤り率でなく、等しい誤り率を与える2つの遅延量(例えば図12の D_3 、 D_5)の中間値を最適な遅延量として設定するようにしてもよい。

【0110】また、表示器に設けたスイッチ等の入力手段を操作することによって、被測定データ信号の最適スレッシュホールド電圧を設定する一連の動作を開始し、その動作が終了した後、最適な遅延量を設定する動作を行ない、設定されたスレッシュホールドレベルと遅延量とを表示器に表示するようにしてもよい。

【0111】また、前記第3の実施例では、クロック信号側の位相を遅延させていたが、これは本発明を限定するものでなく、例えば図14に示すように、可変遅延器71を、被測定データ信号側の入力端子51とレベルシフタ52の間に設けてもよい。また、可変遅延器71をレベルシフタ52とコンパレータ60の間、あるいは、コンパレータ60と識別器72の間に設けてもよい。

【0112】また、前記第3の実施例では、図1に示した波形整形回路10と同一構成の波形整形回路50によって、入力信号の波形整形を行っていたが、シフト量のホールド機能と中間電圧検出回路55の動作停止機能を有する第2の実施例(図5)の波形整形回路10'を用いてもよい。また、同様に図5の変形例としての前述の図6、図7に示したリミッタ機能を有する回路を用いてもよい。

【0113】また、前述した図13の回路をさらに図15のように変形して、前述の図8で説明したデジタル型のホールド回路を形成してもよい。

【0114】この構成の、演算制御部90は、波形整形

回路50のループが安定して最適なシフト量になったことを自ら判定して、ホールド信号(停止信号)をスイッチ回路35および停止回路69へ出力し、最適なシフト量をレベルシフタ52へ固定設定するとともに、中間電圧検出回路55の検出動作を停止させる(なお、停止回路69は、前述の停止回路29と同様の構成からなる)。

【0115】なお、このように、レベルシフタ52への最適シフト量の設定制御および中間電圧検出動作の停止制御を行なう演算制御部90と、可変遅延器71に対する最適遅延量の設定制御を行なう制御部80とを、1つのCPUで構成しておけば、簡単なキー操作等によって、被測定データ信号に対する最適シフト量の設定処理と最適遅延量の設定処理とを一連のプログラムによって連続して行なわせることができ、しかも、他装置とのデータの授受をCPUの通信機能を用いて簡単に行なうことができるという利点がある。

【0116】図16は本発明の第3の実施例の誤り測定装置のより具体的な例を示し、特に、超高周波の被測定データ信号の誤り測定を行なう装置の例である。

【0117】図16において、波形整形回路101に加えられる入力データおよび可変遅延器102に加えられる入力クロックは、それぞれ上述したように適正化されて識別器103に出力される。

【0118】この識別器103で上述したような識別がなされたデータは、 $1/N$ デマルチプレクサ104において、可変遅延器102の出力クロックに基づいてタイミング発生部105から発生する $1/N$ クロックによって、 $1/N$ にデマルチプレクスされる。例えば、入力データが10GHzで $N=32$ の場合、入力データは、310MHzにデマルチプレクスされて32チャンネルデータとしてエラー検出部106でエラー検出される。このエラー結果は、エラー計数部107を介して表示部108および同期制御部109に送られる。基準パターン発生部110は、この同期制御部109からの出力に従ってエラー検出部106に与えるための基準パターンデータを発生する。

【0119】このエラー検出部106、基準パターン発生部110およびエラー計数部107、同期制御部109は、タイミング発生部105からの $1/N$ クロックにより制御される。CPUで構成される制御部111は各部を制御する。なお、オートサーチ部112は、制御部111の制御の下に波形整形回路101および可変遅延器102を前記各実施例と同様にそれぞれ適正な状態に制御する。

【0120】この誤り測定装置では、前記実施例と同様に識別器103で最適のタイミングで識別されたデータ信号が、 $1/N$ の速度の並列データに分割されてエラー判定されるため、超高周波のデータ信号の誤り測定を確実に行なうことができる。

【0121】なお、上記実施例は、本発明のデジタル信号解析装置を誤り測定装置に適用した例について説明したが、ロジックアナライザ等の他のデジタル解析装置にも同様に適用できる。

【0122】

【発明の効果】以上説明したように、本発明の波形整形回路は、入力デジタル信号の直流オフセット電圧すなわち、レベルシフタの出力信号のハイレベル電圧とローレベル電圧との中間の電圧を、所定のしきい値に近づける方向にレベルシフタのシフト量を制御し、そのレベルシフタの出力信号を所定のしきい値で波形整形するように構成されている。

【0123】このため、煩しい波形観測や手動調整をすることなしに、コンパレータに入力されるデジタル信号の振幅の中心が、常に所定のしきい値に一致した状態に追従まれ、確実な波形整形を行なうことができる。

【0124】また、レベルシフタに対する誤差信号の大きさを保持する保持回路と、中間電圧検出回路の動作を停止させる停止手段を設けた波形整形回路では、シフト量を適正量に固定することができ、信号路の高周波特性を悪化させずに済むという効果がある。

【0125】また、本発明のデジタル信号解析装置は、前記説明のように、前記波形整形回路から出力されるデジタル信号とクロック信号との位相を相対的に所定範囲遅延可変して得られた誤り測定結果に基づいて、コンパレータから識別器へ入力されるデジタル信号の隣り合う状態遷移点の間の最適位置に、識別のタイミングが入るための遅延量を検出し、その遅延量を、可変遅延器に設定するように構成されている。

【0126】このため、波形観測をしながらの煩雑な手動による電圧調整や位相調整操作をせずに、コンパレータによる波形整形の動作点や識別タイミングを、波形の乱れによる誤差や個人差のない状態で、最適状態に設定することができる。

【図面の簡単な説明】

【図1】本発明の第1の実施例構成を示すブロック図である。

【図2】図1の要部の具体的な回路の一例を示す回路図である。

【図3】図1の要部の具体的な回路の一例を示す回路図である。

【図4】一実施例の動作を説明するための信号図である。

【図5】本発明の第2の実施例の構成を示すブロック図である。

【図6】第2の実施例の要部の変形例を示す回路図である。

【図7】第2の実施例の要部の変形例を示す回路図である。

【図8】第2の実施例の要部の変形例を示す回路図であ

る。

【図9】第1、第2の実施例の要部の変形例を示す回路図である。

【図10】シフト量を直接読みとるための回路図である。

【図11】本発明の第3の実施例の構成を示すブロック図である。

【図12】第3の実施例の動作を説明するための図である。

【図13】第3の実施例の変形例を示す要部ブロック図である。

【図14】第3の実施例の他の変形例を示すブロック図である。

【図15】第3の実施例の他の変形例を示すブロック図である。

【図16】第3の実施例の要部をより具体的に示したブロック図である。

【図17】従来装置の構成を示すブロック図である。

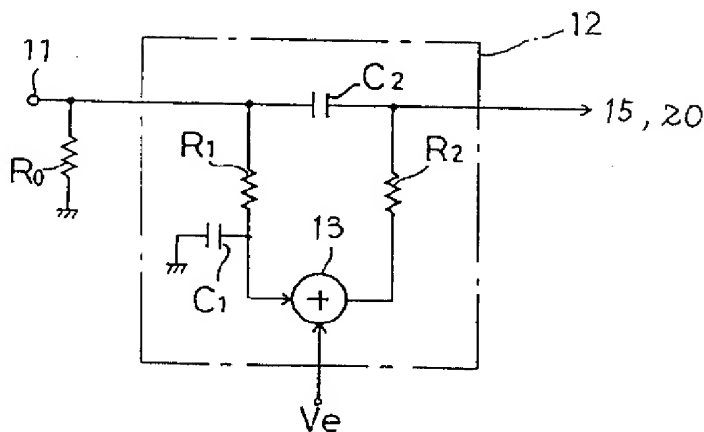
【図18】従来装置の動作を説明するための信号図である。

【符号の説明】

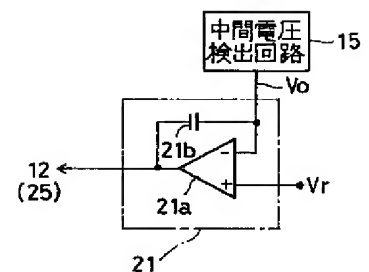
10、10' 波形整形回路
12 レベルシフタ
15 中間電圧検出回路
16 最大値検出回路
17 最小値検出回路
18 中間電圧出力回路
20 コンパレータ
21 制御回路
22 減算器
23 低域通過フィルタ
25 ホールド回路
26、27 スイッチ
29 停止回路

32 A/D変換器
33 メモリ回路
34 D/A変換器
35 スイッチ
37 電圧計
50 波形整形回路
52 レベルシフタ
55 中間電圧検出回路
60 コンパレータ
61 第1の制御回路
65 A/D変換器
71 可変遅延器
72 識別器
75 誤り測定部
76 基準データ発生器
77 符号比較器
78 不一致カウンタ
79 クロックカウンタ
80 制御部
81 表示器
90 演算制御部
101 波形整形回路
102 可変遅延器
103 識別器
104 1/Nデマルチプレクサ
105 タイミング発生部
106 エラー検出部
107 エラー計数部
108 表示部
109 同期制御部
110 基準パターン発生部
111 CPU
112 オートサーチ部

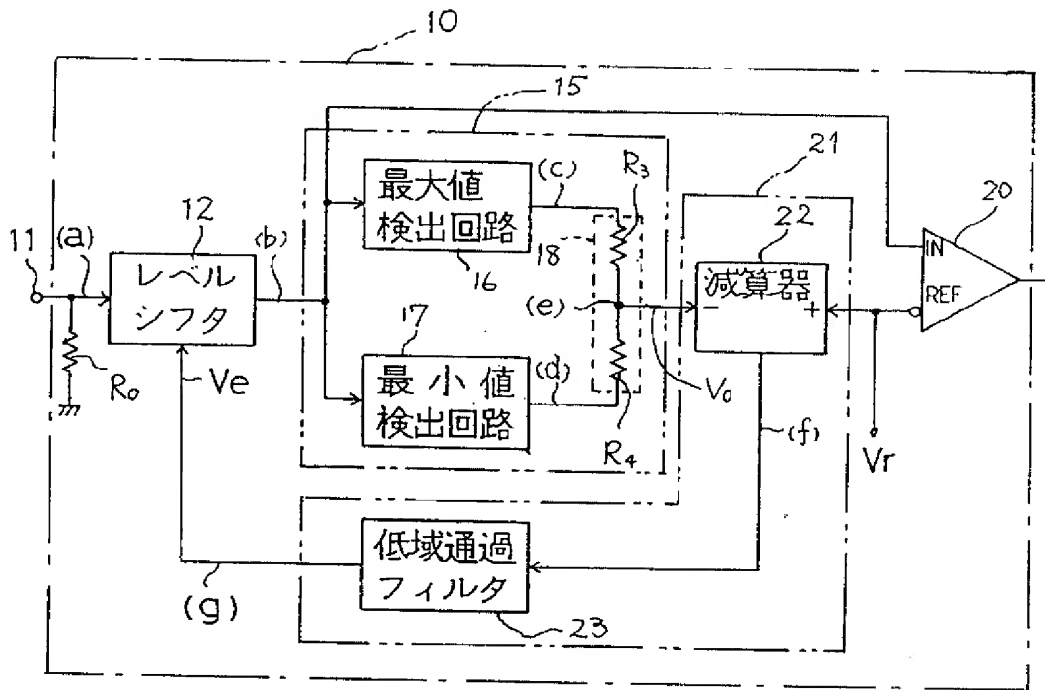
【図2】



【図9】

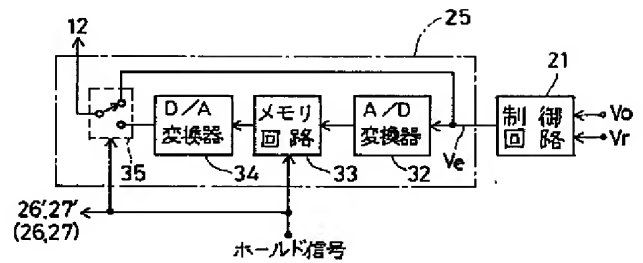
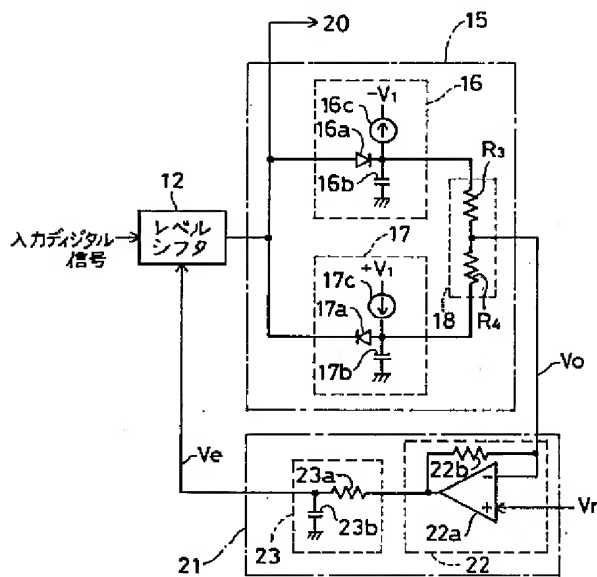


【図1】

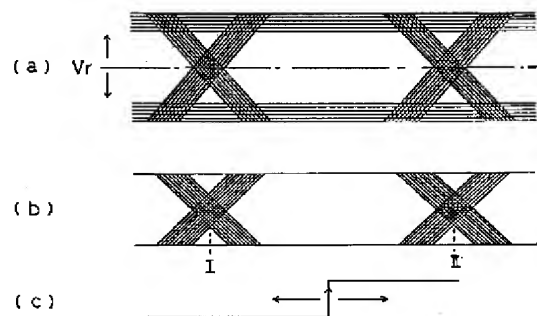


【図3】

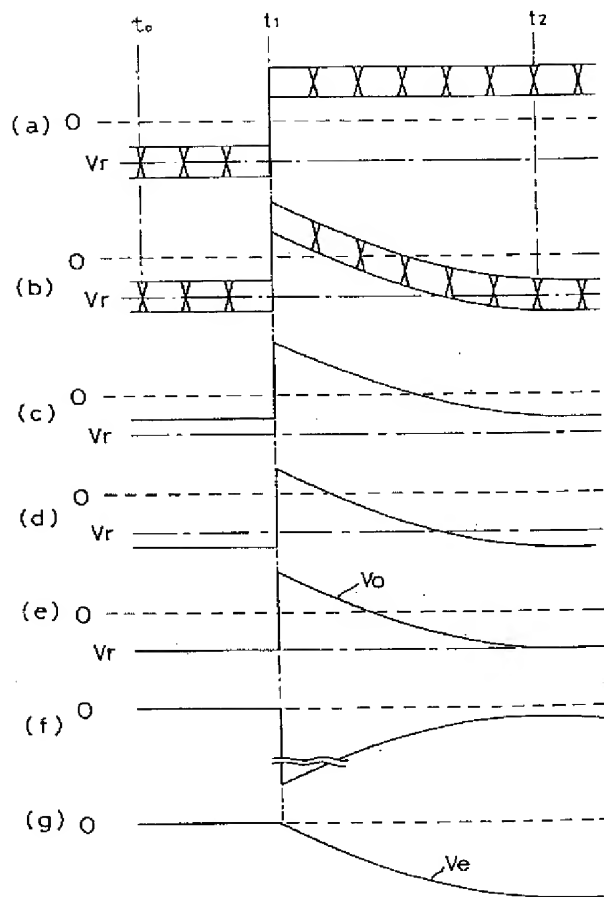
【図8】



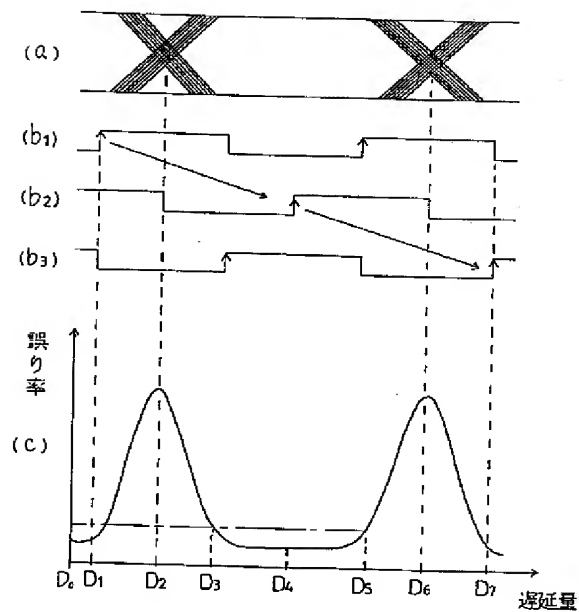
【図18】



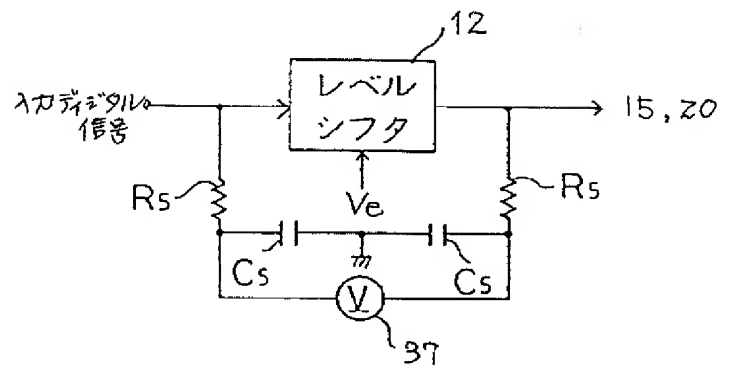
【図4】



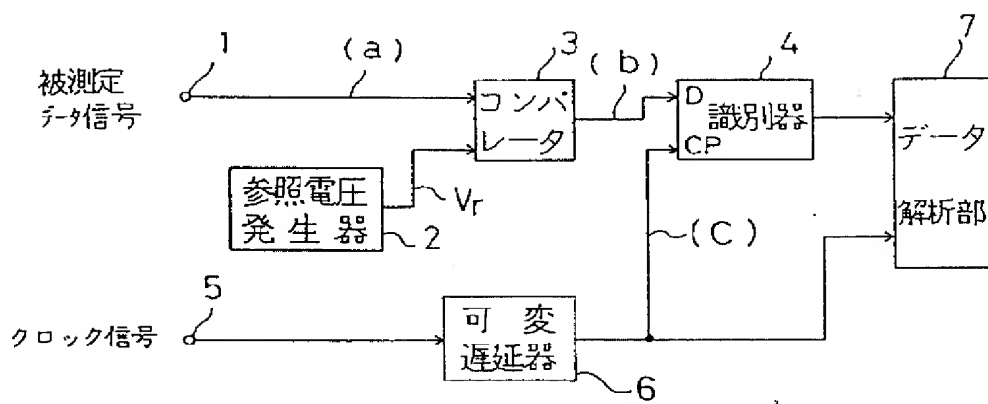
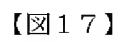
【図12】



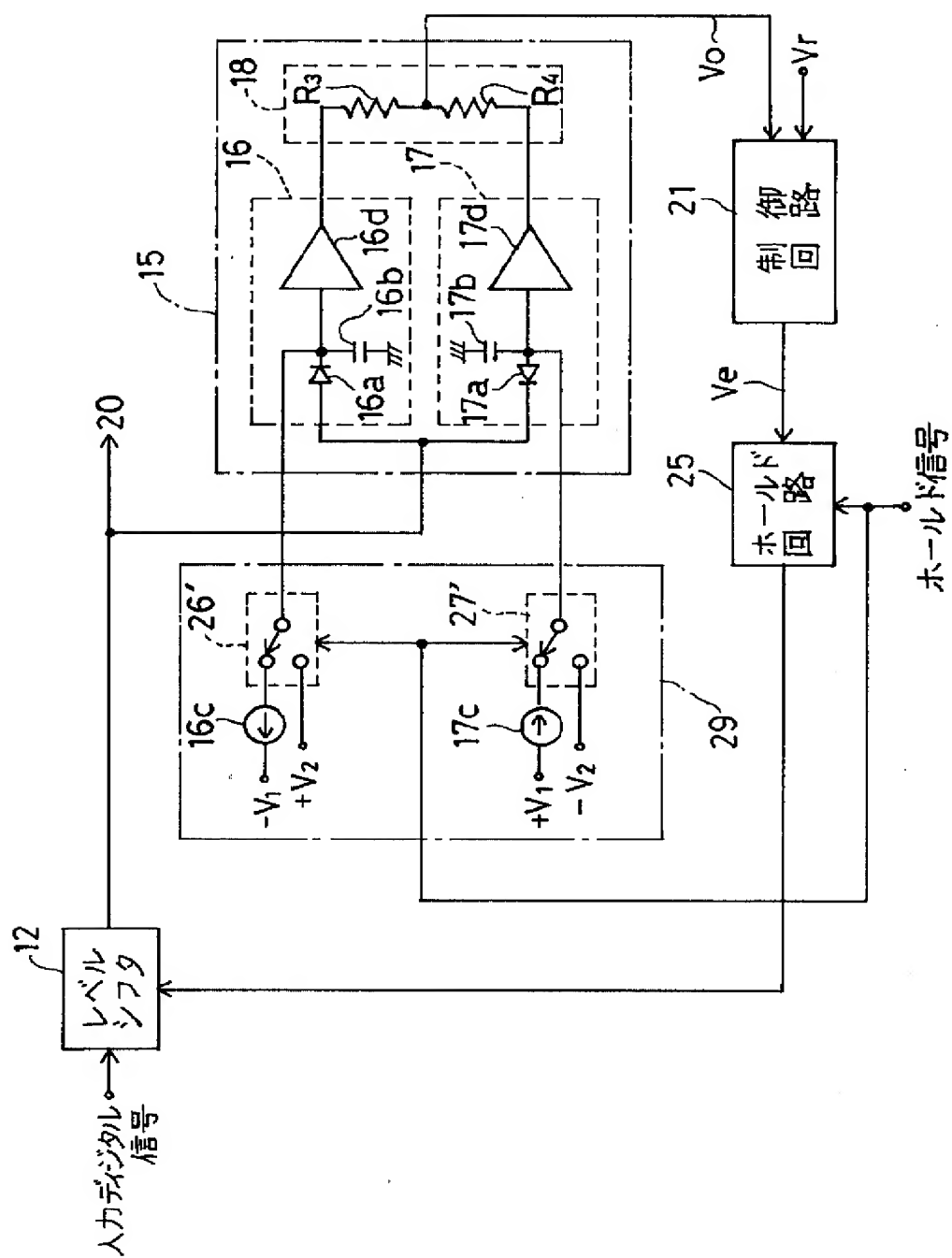
【図10】



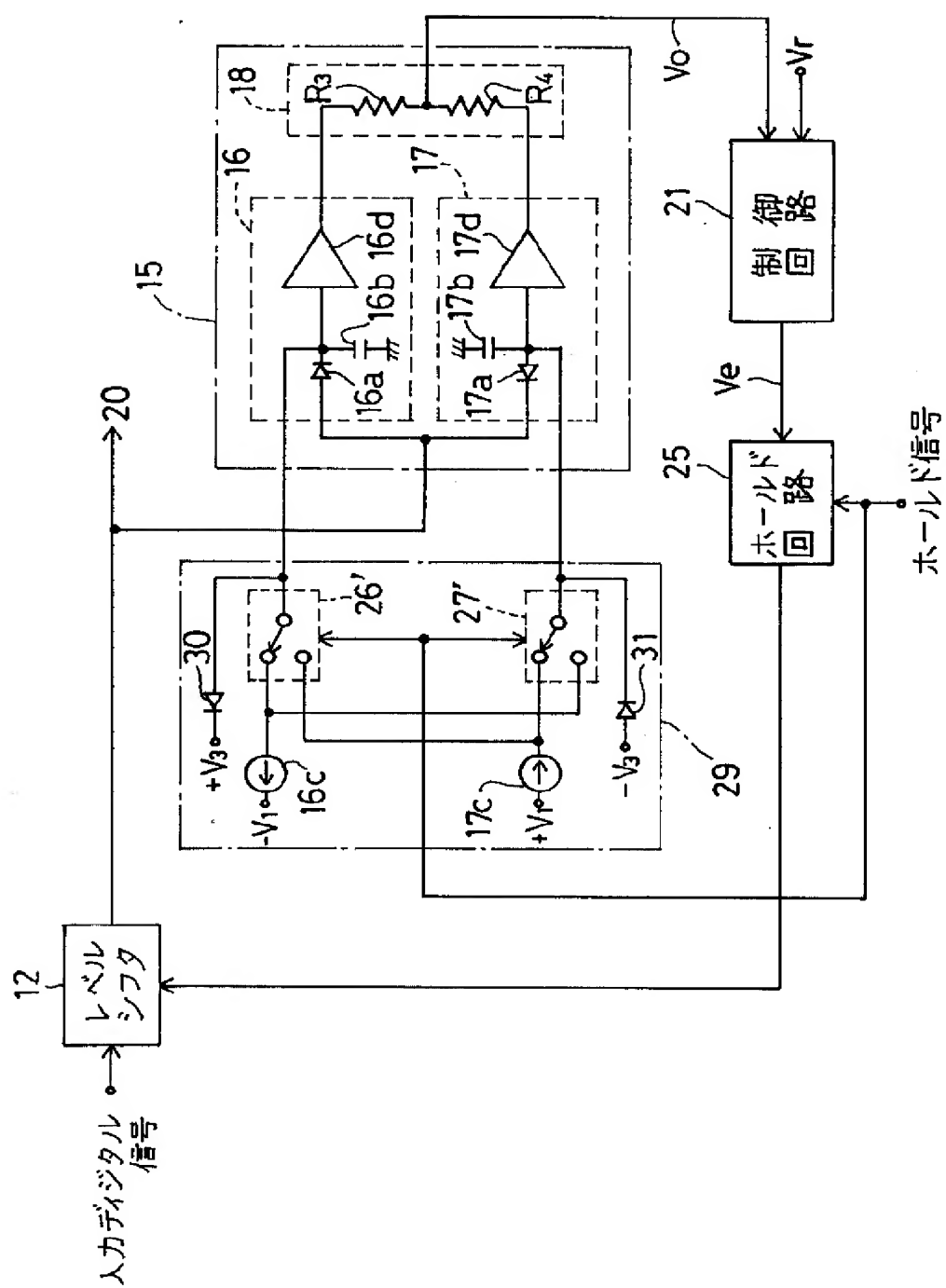
10'



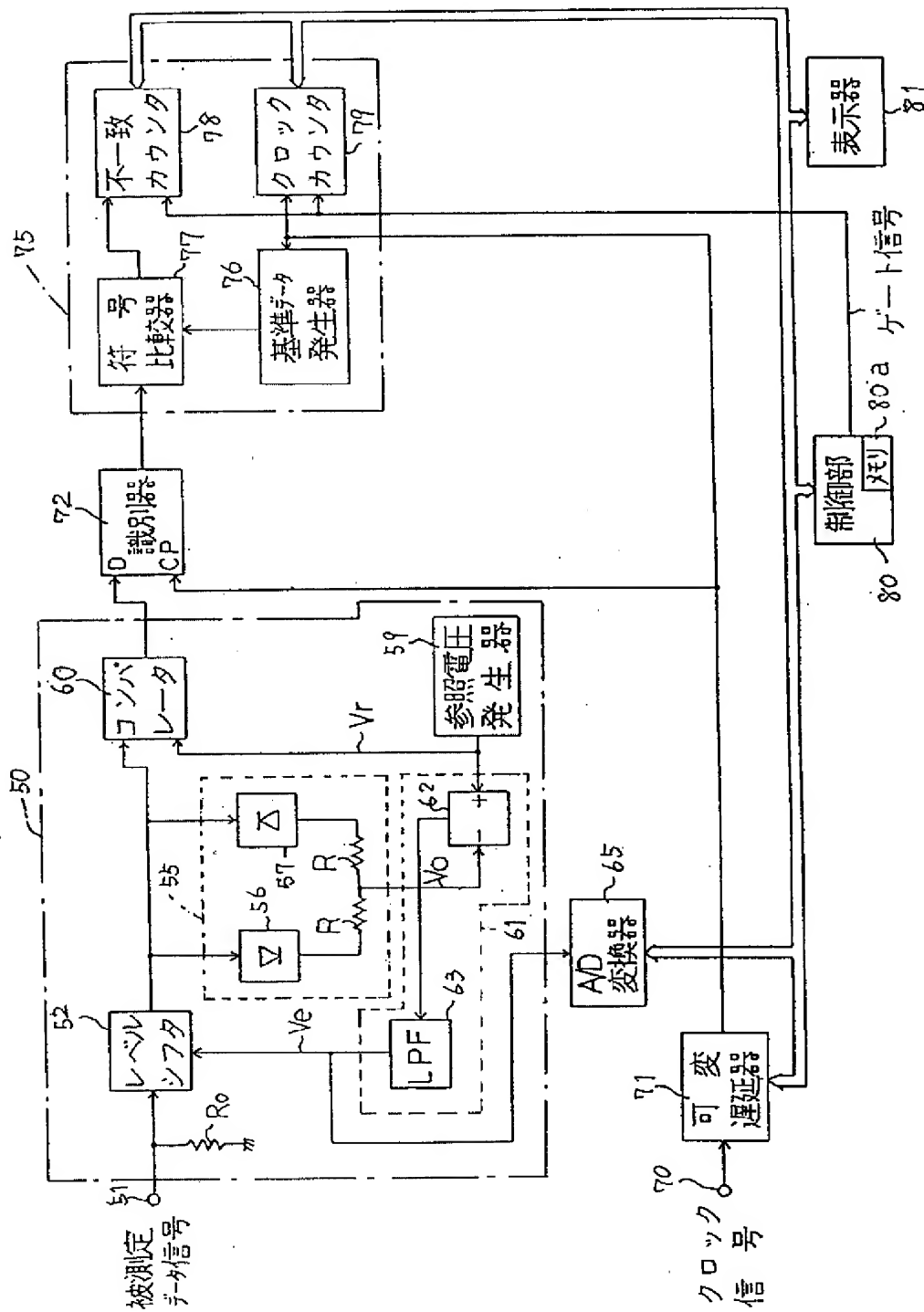
【図6】



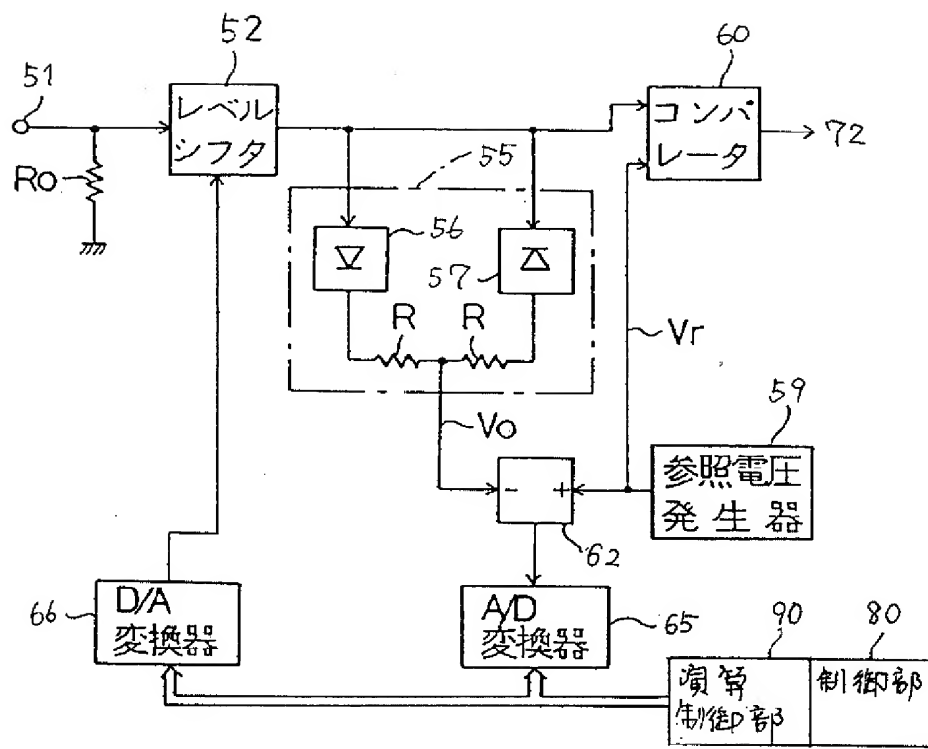
【图7】



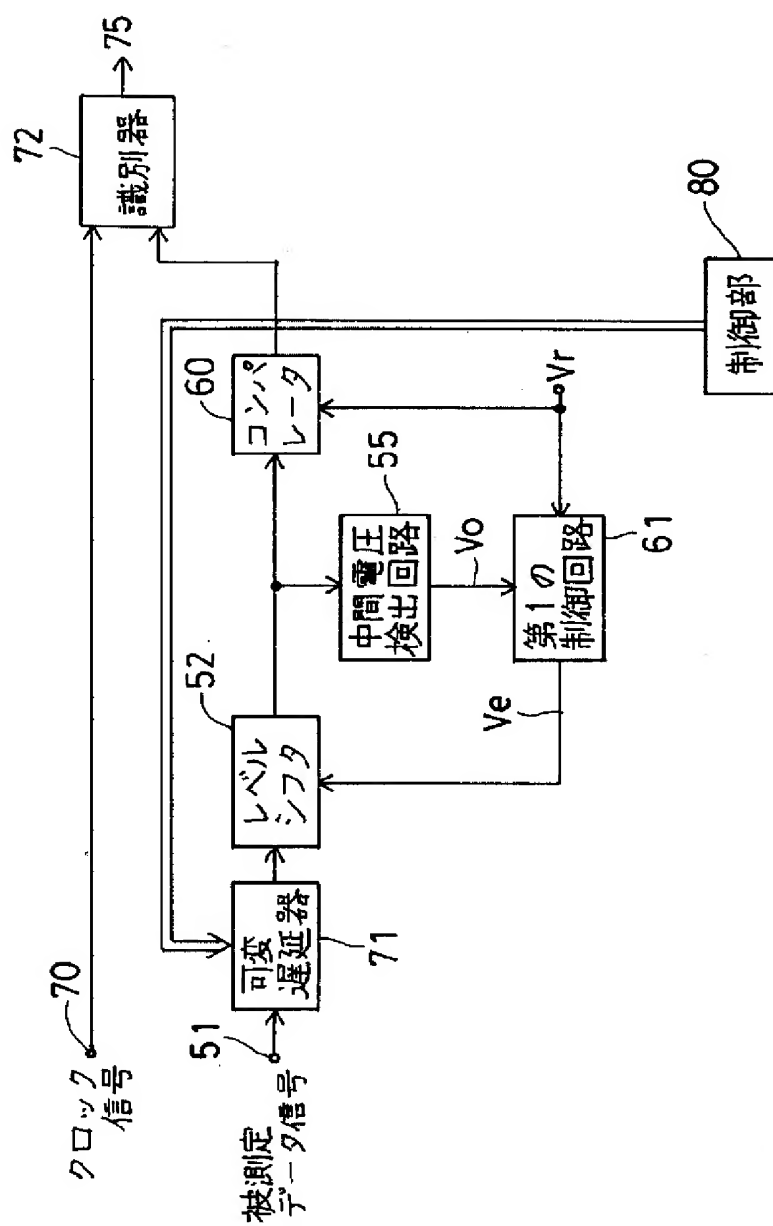
【図11】



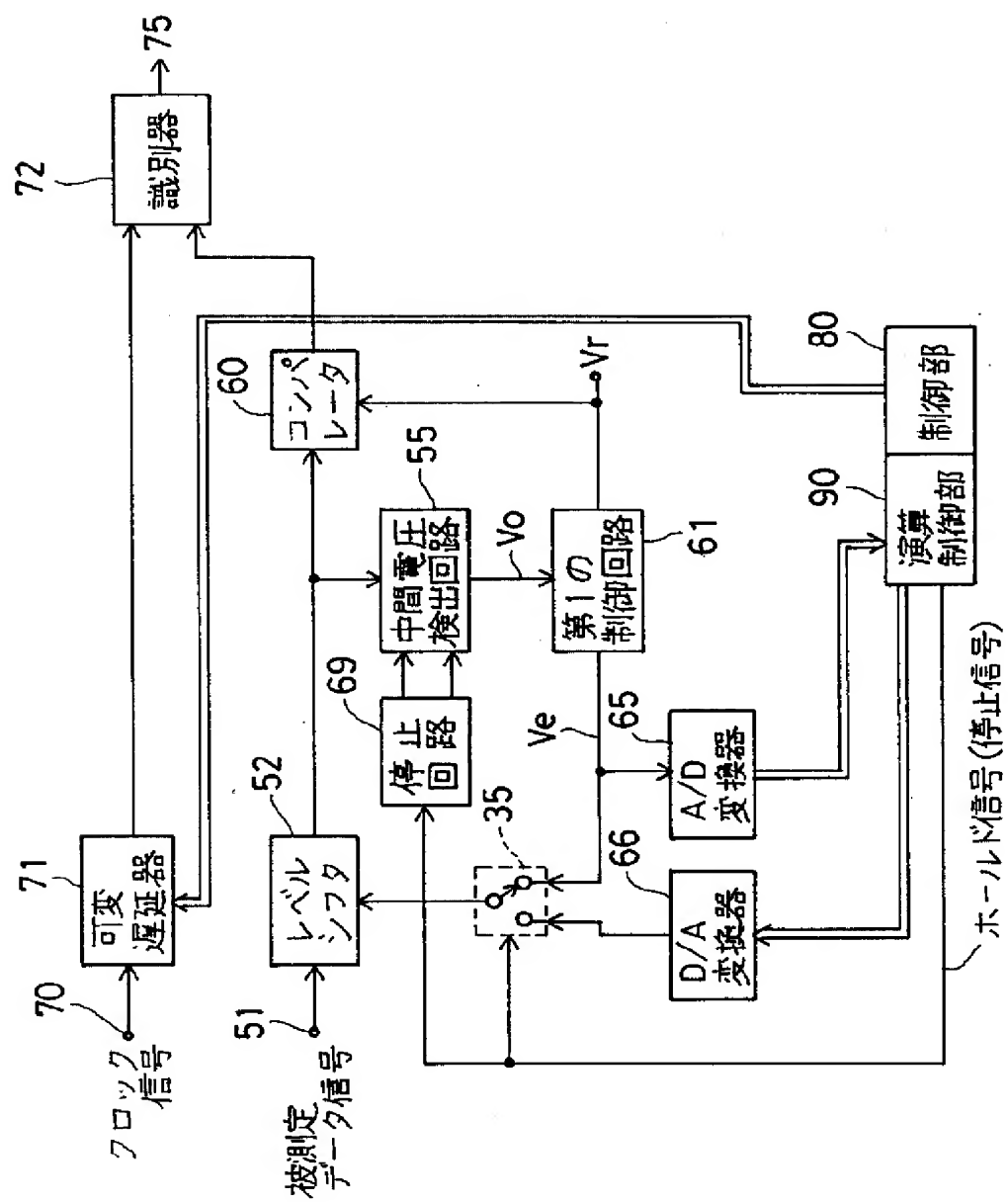
【図13】



【図14】



【図 15】



【図16】

